User Manual

for the Mother Boards:

886LCD/ATX(GV)

886LCD/ATXU(GV)

Document revision history.

Revision	Date	By	Comment
E	Jan. 14th 2009	MLA	Minor corrections. PXE/RPL selection added to BIOS.
D	May 30th 2008	MLA	Battery type updated and Battery load information added.
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B	June 6th, 2006	MLA	Many minor corrections.
1.0	Mar 13th, 2006	PJA	Release version.
0.1	Dec 9th, 2005	PJA	First preliminary manual version.

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Before Contacting Support: Please be prepared to provide as much information as possible:

- CPU Board
  1. Type.
  2. Part-number (Number starting with "6").
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup in the Kontron Section).
  4. BIOS Settings different than *Default* Settings (Refer to the Software Manual).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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1. Introduction

This manual describes the 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards made by KONTRON Technology A/S. The boards will also be denoted 886LCD-GV family if no differentiation is required.

All boards are to be used with the Intel® Pentium® 4, Intel Celeron® and Intel® Celeron® D Processors.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the 886 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 2 before switching-on the power.

2. Installation procedure

2.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has CPU, DDR DRAM and Cooler mounted. In this case Step 2-4 can be skipped.

1. Turn off the power supply.

Warning: Do not use Power Supply without voltage monitoring watchdog, which is standard feature in ATX Power Supplies.
Running the board without 3.3V connected will damage the board after a few minuttes.

2. Insert the DIMM DDR 184pin DRAM module(s). Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR DRAM modules contact your Distributor or FAE.
   DIMM 184pin DRAM modules are supported.

3. Install the processor. The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. Intel® Pentium® 4, Celeron® and Celeron® D processors are supported.

4. Use heat paste or adhesive pads between CPU and cooler and connect the Fan electrically to the FAN3 connector. (See chapter 4.1 for identifying the FAN3 connector).

5. Insert all external cables for hard disk, keyboard etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to flat panel support (with ADD-DVO module). To achieve UDMA-66/100/133 performance on the IDE interface, 80poled UDMA cables **must** be used.

6. Connect power supply to the board by the ATXPWR connector.

7. Turn on the ATX power supply.

8. The PWRSW must be toggled to start the Power supply; this is done by shorting pins pins 19 and 21 on the CN5 connector (see Connector description). A “normally open” switch can be connected via the CN5 connector.

9. Enter the BIOS setup by pressing the “F2” key during boot up. Refer to the Software Manual for details on BIOS setup.

Note: To clear all CMOS settings, including Password protection, move the JP6 jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

2.2 Requirement according to EN60950:

Users of 886LCD-GV boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Component main data

The table below summarises the features of the 886LCD-GV embedded motherboards.

Form factor	886LCD/ATXU(GV): uATX (244,1 x 305,0 mm) 886LCD/ATX(GV): ATX (190,5 x 304,0 mm)
Processor	• Support for Intel® Pentium® 4, Intel Celeron® and Intel® Celeron® D Processors in mPGA478 socket with 400MHz/ 533MHz system bus. • 0.13 micron and 90nm Architecture support • L2 cache: 128KB, 256KB and 512KB
Memory	• 2x184pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets. • Support for DDR 266 (PC2100). DRAM supporting higher speeds: DDR 333 (PC2700) and DDR 400 (PC3200) may be used after qualification testing. • Support for up to 2GB of system memory • ECC not supported
Chipset	Intel 845GV Chipset consisting of: • Intel® 82845GV Graphics and Memory Controller Hub (GMCH) • Intel® 82801DB I/O Controller Hub 4 (ICH4) • 4 Mbit Firmware Hub (FWH) for BIOS
Video	• Intel Extreme Graphics controller • Video memory support: maximum 64MB with more than 128MB DDR SDRAM installed. • The GMCH has an integrated 350 MHz RAMDAC that can directly drive a progressive scan analog monitor up to a resolution of 2048x1536 at 60 Hz. • The GMCH provides two multiplexed Digital Video Out Ports (DVOs) through the onboard AGP 2.0, 1.5V connector that are can drive a 165 MHz pixel clock. o DVI DVO ADD, CRT DVO ADD and LVDS DVO ADD cards supported Note: Only ADD cards are supported , AGP cards are not supported.
Audio	Audio, AC97 version 2.3 subsystem using the Realtek ALC655 codec • Line-out • Line-in • CDROM in • Microphone
I/O Control	Winbond W83627HG LPC Bus I/O Controller
Peripheral interfaces	• USB host interface; 3 host controllers and supports 6 USB ports; includes a EHCI high-speed 2.0 USB controller. USB legacy keyboard function supported. • Two Serial ports (RS232). Port 2 can be set to operate in normal, IrDA or ASKIR mode • One Parallel port, SPP/EPP/ECP • One Floppy port • Two Serial ATA 150 IDE interfaces. • Two Parallel ATA IDE interfaces with UDMA 33, ATA-66, ATA-100 support • PS/2 keyboard and mouse ports • Game/Midi port
LAN Support	1x 10/100Mbits/s LAN subsystem using the Realtek RTL8100C LAN controllers. PXE netboot supported. Wake On LAN (WOL) supported.
BIOS	• Kontron Technology / AMI BIOS (core version 8.00) • Support for Advanced Configuration and Power Interface (ACPI 1.0, 2.0), Plug and Play o Suspend To Ram o Suspend To Disk • SW Watchdog not supported by BIOS • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • SATA RAID Support (RAID modes 0 and 1)

Instantly Available PC Technology	• PCI Rev 2.2 compliant with support for 33 MHz PCI operations • Suspend to RAM support

Expansion Capabilities	• PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.2)
	  • 3 x PCI bus with Bus master mode on 886LCD/ATXU(GV) board
	  • 6 x PCI bus with Bus master mode on 886LCD/ATX(GV) board
	• 2 x DVO ports for ADD card expansion
	• LPC Bus routed to CN7 connector / Trusted Platform Module Header

Hardware Monitor Subsystem	• Fan monitoring: CPU FAN, CHASSIS FAN, PWR FAN • Thermal monitoring: CPU die temperature, System temperature and External temperature input (routed to JP3 connector). • Voltage monitoring • Intrusion detect input (JP6) • SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows)
Operating Systems Support	• WinXP • Win2000 • Win2003 • WinXP Embedded (limitations may apply) • WinCE.net (limitations may apply) • Linux: Feodora Core 3, Suse 9.2 (limitations may apply)
Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. **Storage**: -20°C – 70°C and 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 129679 hours (14,5 years). Calculation based on Telcordia SR-332 method. **Restriction of Hazardeous Substances (RoHS):** 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards are RoHS compliant. **Capacitor utilization:** No Tantal capacitors on board. Only Japanese brand Aluminium capacitors rated for 100 ºC used on board.
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / PN CR2032NL/LE or CR-2032L/BE. Expected minimum 5 years retention varies depending on temperature, actual application on/off rate and variation within chipset and other components. Approximately current draw is 3.7µA (no PSU connected). **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

3.2 Processor support table.

886LCD/ATX(GV) and 886LCD/ATX(GV) boards are designed to support the following processors:
Intel® Pentium® 4 Processors
Intel® Celeron® D Processors
Intel Celeron® Processors

Speed	Cache size	Intel Single Pack Product Order Code	Intel OEM Product Order Code
Intel® Pentium 4® Embedded Processors			
2.0A GHZ 400MHz FSB	512K		RK80532PC041512
2.40 GHZ 533MHz FSB	512K		RK80532PE056512
2.60 GHZ 400MHz FSB	512K		RK80532PC064512
2.80 GHZ 400MHz FSB	512K		RK80532PE072512
Intel® Celeron® Embedded Processors			
2.00 GHZ, 400MHz FSB	128K		RK80532RC041128
2.50 GHZ, 400MHz FSB	128K		RK80532RC060128
Intel® Celeron® D Embedded Processors			
2.80 GHz, 533MHz FSB	256K	BX80546RE2800C	RK80546RE072256
Intel® Pentium 4® Processors			
1.60 GHZ, 400MHz FSB	512K		RK80534PC025512
1.60 GHZ, 400MHz FSB	512K	BX80532PC1600D	
1.80 GHZ, 400MHz FSB	512K		RK80534PC033512
1.80 GHZ, 400MHz FSB	512K	BX80532PC1800D	RK80532PC033512
2.00 GHZ, 400MHz FSB	512K	BX80532PC2000D	RK80532PC041512
2.20 GHZ, 400MHz FSB	512K	BX80532PC2200D	RK80532PC049512
2.26 GHZ, 533MHz FSB	512K	BX80532PE2266D	RK80532PE051512
2.40 GHZ, 400MHz FSB	512K	BX80532PC2400D	RK80532PC056512
2.40 GHZ, 533MHz FSB	512K	BX80532PE2400D	RK80532PE056512
2.50 GHZ, 400MHz FSB	512K	BX80532PC2500D	RK80532PC060512
2.53 GHZ, 533MHz FSB	512K	BX80532PE2533D	RK80532PE061512
2.60 GHZ, 400MHz FSB	512K	BX80532PC2600D	RK80532PC064512
2.66 GHZ, 533MHz FSB	512K	BX80532PE2667D	RK80532PE067512
2.80 GHZ, 533MHz FSB	512K	BX80532PE2800D	RK80532PE072512
3.06 GHZ, 533MHz FSB, HT*	512K	BX80532PE3066D	RK80532PE083512
Intel® Celeron® Processors			
1.70 GHZ, 400MHz FSB	128K	BX80531P170G128	RK80531RC029128
1.80 GHZ, 400MHz FSB	128K	BX80531P180G128	RK80531RC033128
2.00 GHZ, 400MHz FSB	128K	BX80532RC2000B	RK80532RC041128
2.10 GHZ, 400MHz FSB	128K	BX80532RC2100B	RK80532RC045128
2.20 GHZ, 400MHz FSB	128K	BX80532RC2200B	RK80532RC049128
2.30 GHZ, 400MHz FSB	128K	BX80532RC2300B	RK80532RC052128
2.30 GHZ, 400MHz FSB	128K		B80532RC052128
2.40 GHZ, 400MHz FSB	128K	BX80532RC2400B	RK80532RC056128
2.50 GHZ, 400MHz FSB	128K	BX80532RC2500B	RK80532RC060128
2.60 GHZ, 400MHz FSB	128K	BX80532RC2600B	RK80532RC064128
2.70 GHZ, 400MHz FSB	128K	BX80532RC2700B	RK80532RC068128
2.80 GHZ, 400MHz FSB	128K	BX80532RC2800B	RK80532RC072128

Speed	Cache size	Intel Single Pack Product Order Code	Intel OEM Product Order Code
Intel® Celeron® D Processors			
3.20 GHz, 533MHz FSB	256K	BX80546RE3200C	RK80546RE088256
3.06 GHz, 533MHz FSB	256K	BX80546RE3066C	RK80546RE083256
2.93 GHz, 533MHz FSB	256K	BX80546RE2933C	RK80546RE077256
2.80 GHz, 533MHz FSB	256K	BX80546RE2800C	RK80546RE072256
2.66 GHz, 533MHz FSB	256K	BX80546RE2667C	RK80546RE067256
2.53 GHz, 533MHz FSB	256K	BX80546RE2533C	RK80546RE061256
2.40 GHz, 533MHz FSB	256K	BX80546RE2400C	RK80546RE056256
2.26 GHz, 533MHz FSB	256K	BX80546RE2267C	RK80546RE051256
2.13 GHz, 533MHz FSB	256K	BX80546RE2130C	RK80546RE046256

* HT = Hyper Threading support

3.3 System Memory support

The 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards have two onboard DIMM sockets and support the following memory features:

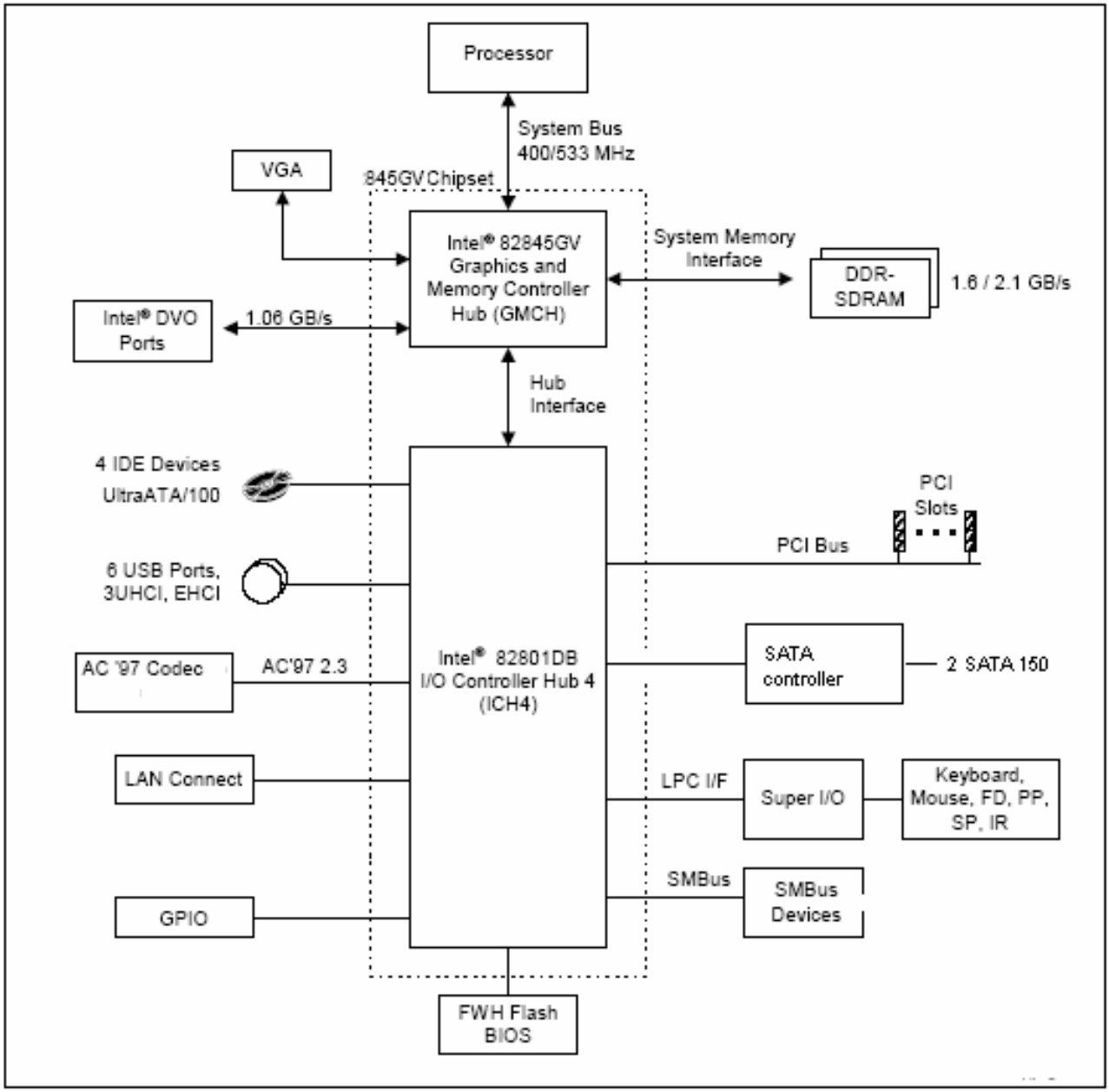
- 2.5V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Supports up to two single-sided and/or double-sided DIMMs (four rows populated) with unbuffered PC1600/PC2100 DDR-SDRAM
- Supports 64 Mbit, 128 Mbit, 256 Mbit and 512 Mbit technologies for x8 and x16 width devices.
- Maximum of 2 Gbytes system memory by using 512 Mbit technology devices (double sided)
- Supports 200 MHz and 266 MHz DDR devices
- 64-bit data interface
- ECC not supported with the Intel 845GV chipset

The installed DDR SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

In general DDR SDRAM with higher speeds than 266MHz may be used (e.g. 333MHz or 400MHz), but it is recommended to run a qualification test before use or to use Kontron Technology validated DDR SDRAM.

3.4 System overview

The block diagram below shows the architecture and main components of the 886LCD boards. The two key components on the board are the Intel® 845GV and Intel® ICH4 Embedded Chipsets.



3.5 Power Consumption

This section describes static and dynamic power consumption on the 886LCD/ATXU(GV) board in a specific configuration:

- 886LCD/ATXU(GV)
- P4, 2.0GHz, 400MHz FSB, 256MByte L2 cache
- P4 cooler
- 256Mbyte of PC2100 / 266MHz DDR SDRAM
- VGA monitor, Keyboard and mouse inserted

Wire colour	Yellow (CPU)	Red	Orange	Yellow	Blue	Purple	White	Total Power
Voltage	12,00 V	5,00 V	3,30 V	12,00 V	-12,00 V	5,00 V	-5,00 V	
State	/[A]	/[A]	/[A]	/[A]	/[A]	/[A]	/[A]	/[W]
XP Idle DC	0,74	0,24	2,65	0,34	0,02	0,06	0,03	23,60
XP Idle AC	0,06	0,00	0,05	0,07	0,03	0,04	0,05	2,54
XP Idle power								26,13
XP Full Load DC	3,60	0,29	3,66	0,34	0,03	0,04	0,04	61,57
XP Full Load AC	0,38	0,02	0,29	0,08	0,03	0,04	0,04	7,34
XP Full Load power								68,91

4. Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

.

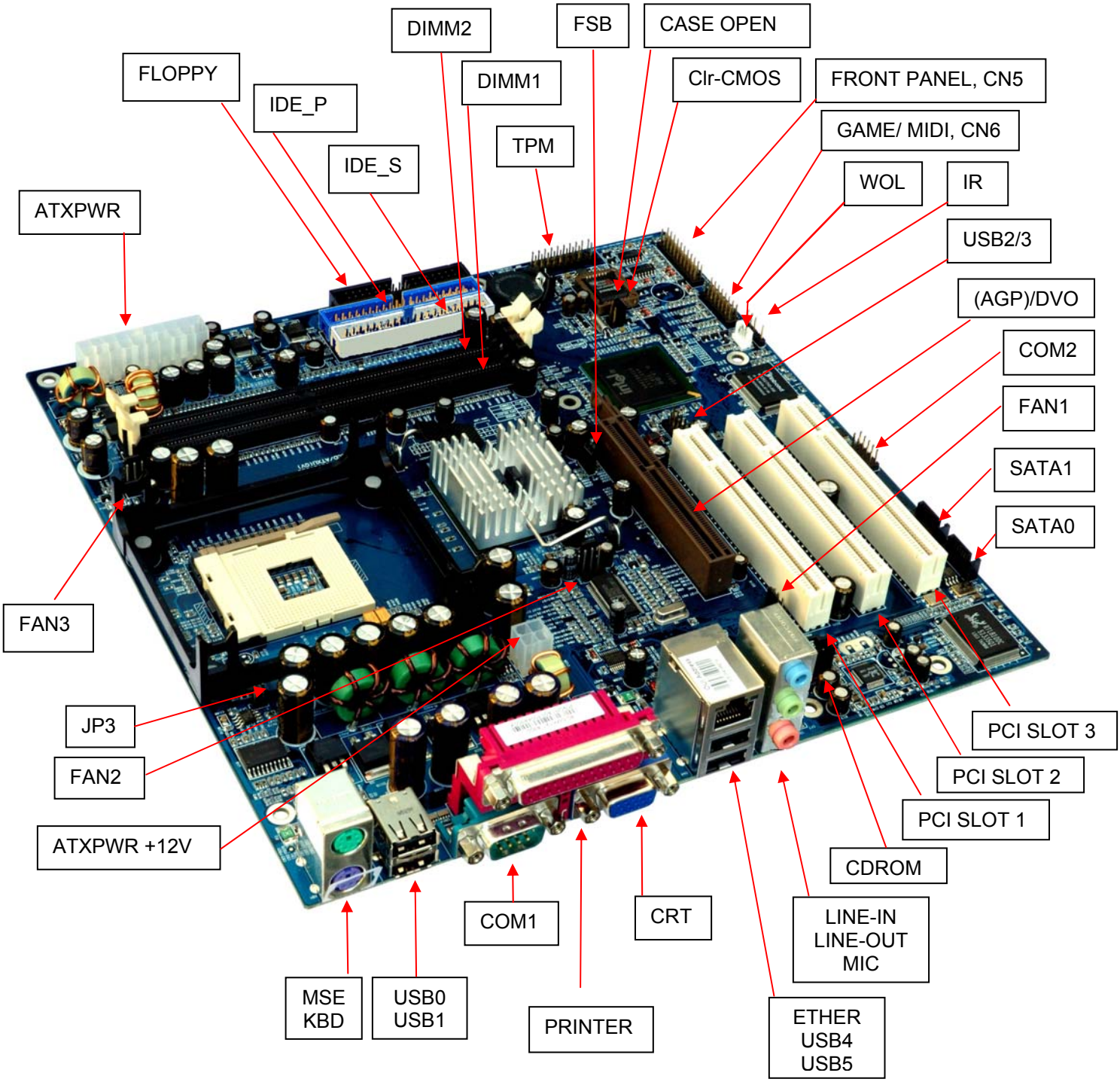
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI : Analog Input. AO : Analog Output. I : Input, TTL compatible if nothing else stated. IO : Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS : Schmitt-trigger input, TTL compatible. IOC : Input / open-collector Output, TTL compatible. NC : Pin not connected. O : Output, TTL compatible. OC : Output, open-collector or open-drain, TTL compatible. OT : Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR : Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

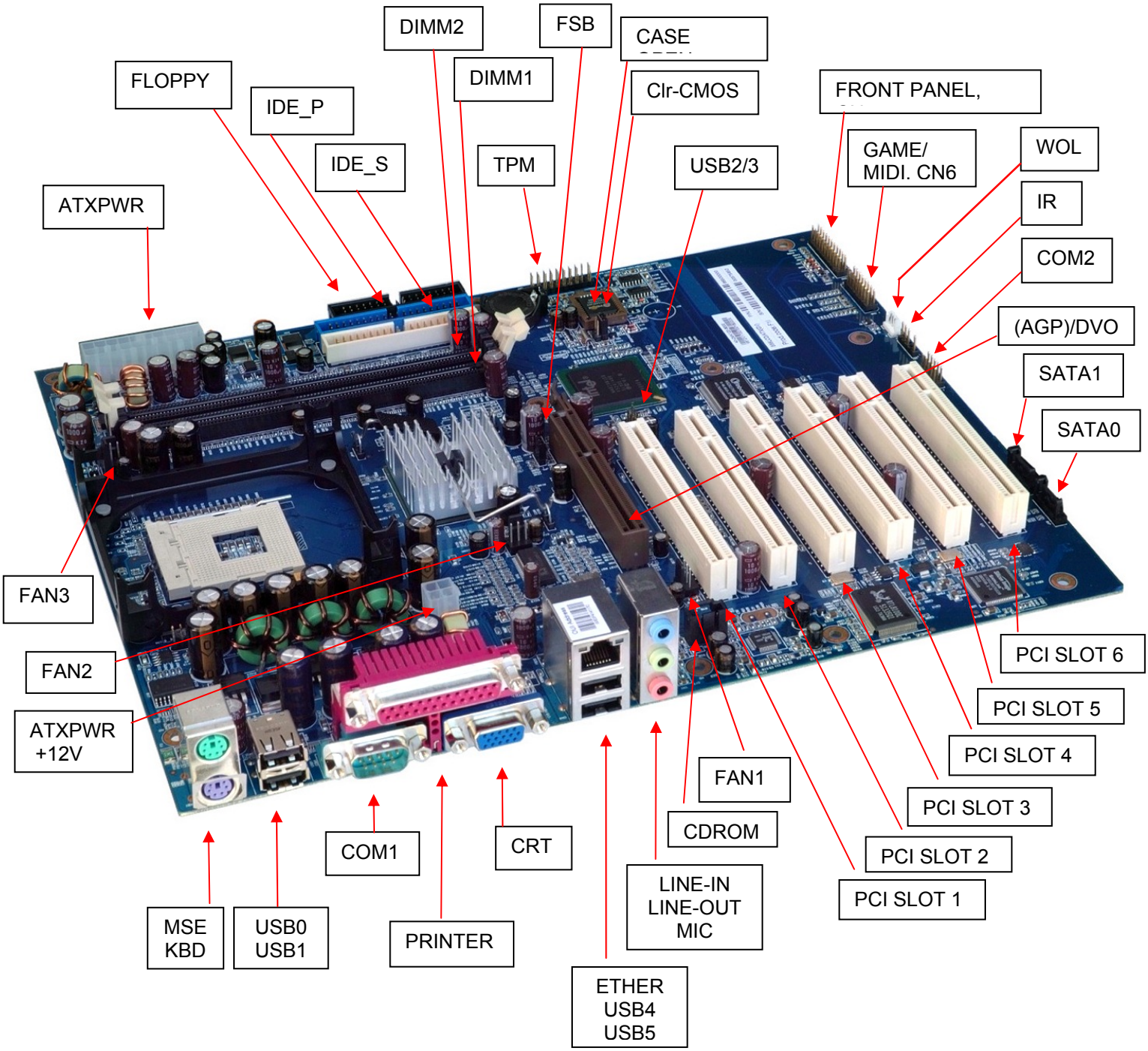
The abbreviation *TBD* (To Be Determined) is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

4.1 Connector layout

4.1.1 886LCD/ATXU(GV)



4.1.2 886LCD/ATX(GV)



4.2 Power Connector (ATXPWR, ATXPWR+12V)

The 886LCD/ATX(GV) and 886LCD/ATXU(GV) is designed to be supplied from a standard ATX power supply.

ATX Power Connector 886LCD/ATX(GV) and 886LCD/ATXU(GV)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	+12V	10	20	5V	PWR	-	-	
	-	-	PWR	SB5V	9	19	5V	PWR	-	-	
	4K7	-	I	P_OK	8	18	-5V	PWR	-	-	1
	-	-	PWR	GND	7	17	GND	PWR	-	-	
	-	-	PWR	5V	6	16	GND	PWR	-	-	
	-	-	PWR	GND	5	15	GND	PWR	-	-	
	-	-	PWR	5V	4	14	PSON#	OC	-	-	
	-	-	PWR	GND	3	13	GND	PWR	-	-	
	-	-	PWR	3V3	2	12	-12V	PWR	-	-	
	-	-	PWR	3V3	1	11	3V3	PWR	-	-	

Note: -5V supply is not used onboard.

+12V Power Connector 886LCD/ATX(GV) and 886LCD/ATXU(GV)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	4	3	+12V	PWR	-	-	
	-	-	PWR	GND	2	1	+12V	PWR	-	-	

The requirements to the supply voltages are as follows (also refer to ATX specification version 2.03):

Supply	Min	Max	Tolerance
3V3	3.14V	3.46V	+/-5%
5V	4.75V	5.25V	+/-5%
SB5V	4.75V	5.25V	+/-5%
+12V	11.4V	12.6V	+/-5%
–12V	–13.2V	–10.8V	+/-10%

Control signal description:

P_OK	Active high signal from the power supply indicating that the 5V and 3V3 supplies are within operating limits. It is strongly recommended to use an ATX supply with the 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from 5V_STB when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6 5	MSCLK	IOC	TBD	2K2	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	MSDAT	IOC	TBD	2K2	
			-	NC	6 5	KBDCLK	IOC	TBD	2K2	
	-	-	PWR	5V/SB5V	4 3	GND	PWR	-	-	
	-	-	-	NC	2 1	KBDDAT	IOC	TBD	2K2	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.4 Display Connectors

The 886LCD board family provides onboard two basic types of interfaces to a display: Analog CRT interface and a digital interface typically used with flat panels. The digital interface to flat panels can be achieved through the DVO port available on the AGP connector by using a dedicated ADD card.

4.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		ANA-GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		ANA-GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	2K7	
						8		ANA-GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		DIG-GND	PWR	-	-	
	-	-	PWR	DIG-GND	5		15	DDCCLK	IO	TBD	2K7	

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.

Signal Description - CRT Connector:

HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

4.4.2 (AGP)/DVO connector

The 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards are equipped with the Intel 845GV chipset. The GV chipset does not support AGP output, but only DVO output.

Note	Type	Signal	PIN		Signal	Type	Note
		OVRCNT	B1	A1	+12V	PWR	
	PWR	+5V	B2	A2	TYPEDET		
	PWR	+5V	B3	A3	RSVD		
		NC	B4	A4	NC		
	PWR	GND	B5	A5	GND	PWR	
		INTB	B6	A6	INTA		
		AGPCLK	B7	A7	RST-		
		GREQ	B8	A8	GGNT		
	PWR	+3.3V	B9	A9	+3.3V	PWR	
		ST0	B10	A10	ST1		
		ST2	B11	A11	RSVD		
	I	RBF	B12	A12	PIPE	I	
	PWR	GND	B13	A13	GND	PWR	
		RSVD	B14	A14	WBF	I	
	I	ADD_ID0	B15	A15	ADD_ID1	I	
	PWR	+3.3V	B16	A16	+3.3V	PWR	
	I	ADD_ID2	B17	A17	ADD_ID3	I	
	I	ADD_RS	B18	A18	ADD_RS		
	PWR	GND	B19	A19	GND	PWR	
	I	ADD_ID4	B20	A20	ADD_ID5	I	
	I	ADD_ID6	B21	A21	ADD_ID7	I	
		RSVD	B22	A22	RSVD		
	PWR	GND	B23	A23	GND	PWR	
	PWR	3V3AUX	B24	A24	RSVD		
	PWR	+3.3V	B25	A25	+3.3V	PWR	
		DVOC_Fld/Stl	B26	A26	DVOBC_Intr-		
		DVOC_D10	B27	A27	DVOC_D11		
	PWR	+3.3V	B28	A28	+3.3V	PWR	
		DVOC_D8	B29	A29	DVOC_D9		
		DVOC_D6	B30	A30	DVOC_D7		
	PWR	GND	B31	A31	GND	PWR	
		DVOC_Clk+	B32	A32	DVOC_Clk-		
		DVOC_D4	B33	A33	DVOC_D5		
	PWR	+1.5V	B34	A34	+1.5V	PWR	
		DVOC_D2	B35	A35	DVOC_D3		
		DVOC_D0	B36	A36	DVOC_D1		
	PWR	GND	B37	A37	GND	PWR	
		DVOC_Hsync	B38	A38	DVOC_Blank-		
		ADD_RS	B39	A39	DVOC_Vsync		
	PWR	+1.5V	B40	A40	+1.5V	PWR	
		M_I2CClk	B41	A41	M_DVI_Data		
		M_I2CData	B46	A46	M_DVI_Clk		
	PWR	+1.5V	B47	A47	M_DDCData		
		GPERR	B48	A48	PME		
	PWR	GND	B49	A49	GND	PWR	
		GSERR	B50	A50	ADD_Detect		
		DVOB_Blank-	B51	A51	M_DDCClk		
	PWR	+1.5V	B52	A52	+1.5V	PWR	
		DVOB_Fld/Stl	B53	A53	DVOBC_ClkInt		
		DVOB_D10	B54	A54	DVOB_D11		
	PWR	GND	B55	A55	GND	PWR	
		DVOB_D8	B56	A56	DVOB_D9		
		DVOB_D6	B57	A57	DVOB_D7		
	PWR	+1.5V	B58	A58	+1.5V	PWR	
		DVOB_Clk+	B59	A59	DVOB_Clk-		
		DVOB_D4	B60	A60	DVOB_D5		
	PWR	GND	B61	A61	GND	PWR	
		DVOB_D2	B62	A62	DVOB_D3		
		DVOB_D0	B63	A63	DVOB_D1		
	PWR	+1.5V	B64	A64	+1.5V	PWR	
		DVOB-Vsync	B65	A65	DVOB_Hsync		
		VREFCG	B66	A66	NC		

Signal Description – (AGP)/DVO Connector:

Signal	Description
DVOB_CLK; DVOB_CLK#	**DVOB Clock Output:** These signals provide a differential pair reference clock that can run up to 165 MHz. Formerly known by: DVOB_CLKOUT0=DVOB_CLK and DVOB_CLKOUT1=DVOB_CLK#. Care should be taken to be sure that DVOB_CLK is connected to the primary clock receiver of the Intel® DVO device.
DVOB_D[11:0]	**DVOB Data:** This data bus is used to drive 12-bit pixel data on each edge of DVOB_CLK(#). This provides 24 bits of data per clock.
DVOB_HSYNC	**Horizontal Sync:** This is the HSYNC signal for the DVOB interface. The active polarity of the signal is programmable.
DVOB_VSYNC	**Vertical Sync:** This is the VSYNC signal for the DVOB interface. The active polarity of the signal is programmable.
DVOB_BLANK#	**Flicker Blank or Border Period Indication:** DVOB_BLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels.
DVOBC_CLKINT#	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to the dot clock PLL (DPLL) for the multiplexed DVO devices. This pin may also be programmed to be an interrupt input for either of the multiplexed DVO devices.
DVOB_FLDSTL	**TV Field and Flat Panel Stall Signal:** This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The polarity is programmable for both modes and the input may be disabled completely.
DVOC_CLK; DVOC_CLK#	**DVOC Clock Output:** These pins provide a differential pair reference clock that can run up to 165 MHz. Formerly known by: DVOC_CLKOUT0=DVOC_CLK and DVOC_CLKOUT1=DVOC_CLK#. Care should be taken to be sure that DVOC_CLK is connected to the primary clock receiver of the DVO device.
DVOC_D[11:0]	**DVOC Data:** This data bus is used to drive 12-bit pixel data on each edge of DVOC_CLK(#). This provides 24 bits of data per clock.
DVOC_HSYNC	**Horizontal Sync:** This is the HSYNC signal for the DVOC interface. The active polarity of the signal is programmable.
DVOC_VSYNC	**Vertical Sync:** This is the VSYNC signal for the DVOC interface. The active polarity of the signal is programmable.
DVOC_BLANK#	**Flicker Blank or Border Period Indication:** DVOC_BLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this signal indicates active pixels excluding the border. When programmed as a border period indication, this signal indicates active pixel including the border pixels.
DVOBC_INTR#	**DVOBC Interrupt:** This signal may be used as an interrupt input for either of the multiplexed DVO devices.
DVOC_FLDSTL	**TV Field and Flat Panel Stall Signal:** This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The polarity is programmable for both modes and the input may be disabled completely.
M_I2CCLK	**MI2C_CLK:** The specific function of this signal is I2C_CLK for a multiplexed digital display. This signal is tri-stated during a hard reset.
M_I2CDATA	**MI2C_DATA:** The specific function of this signal is I2C_DATA for a multiplexed digital display. This signal is tri-stated during a hard reset.
M_DVI_CLK	**MDVI_CLK:** The specific function is DVI_CLK (DDC) for a multiplexed digital display connector. This signal is tri-stated during a hard reset.
M_DVI_DATA	**MDVI_DATA:** The specific function of this signal is DVI_DATA (DDC) for a multiplexed digital display connector. This signal is tri-stated during a hard reset.
M_DDCCLK	**MDDC_CLK:** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector. This signal is tri-stated during a hard reset.
M_DDCDATA	**MDDC_DATA:** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector. This signal is tri-stated during a hard reset.
ADD_ID[7:0]	**ADD Card ID:** These signals will be strapped on the ADD card for software identification purposes. These signals may need pull-up or pull-down resistors in a DVO device down scenario.

4.5 Parallel ATA harddisk interface

Two parallel ATA harddisk controllers are available on the board – a primary and a secondary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary and secondary controller board by means of the 40 pin IDC connectors, IDE_P and IDE_S.

The harddisk controllers support Bus master IDE, ultra DMA 33/66/100 MHz and standard operation modes.

The signals used for the harddisk interface are the following:

DA*2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCS*1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
D*15..8	High part of data bus.
D*7..0	Low part of data bus.
IOR*#	I/O Read.
IOW*#	I/O Write.
IORDY*#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESET*#	Reset signal to the hard disk.
HDIRQ*	Interrupt line from hard disk.
CBLID*	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQ*	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACK*#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACT*#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

"*" is "A" for primary and "B" for secondary controller.
The pinout of the connectors are defined in the following sections.

4.5.1 IDE Hard Disk Connector (IDE_P)

This connector can be used for connection of up till two primary IDE drives.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETA#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	10K	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	/15K		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

4.5.2 IDE Hard Disk Connector (IDE_S)

This connector can be used for connection of up till two secondary IDE drive(s).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETB#	1	2	GND	PWR	-	-	
	-	TBD	IO	DB7	3	4	DB8	IO	TBD	-	
	-	TBD	IO	DB6	5	6	DB9	IO	TBD	-	
	-	TBD	IO	DB5	7	8	DB10	IO	TBD	-	
	-	TBD	IO	DB4	9	10	DB11	IO	TBD	-	
	-	TBD	IO	DB3	11	12	DB12	IO	TBD	-	
	-	TBD	IO	DB2	13	14	DB13	IO	TBD	-	
	-	TBD	IO	DB1	15	16	DB14	IO	TBD	-	
	-	TBD	IO	DB0	17	18	DB15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQB	21	22	GND	PWR	-	-	
	-	TBD	O	IOWB#	23	24	GND	PWR	-	-	
	-	TBD	O	IORB#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYB	27	28	GND	PWR	-	-	
	-	-	O	DDACKB#	29	30	GND	PWR	-	-	
	/10K	-	I	HDIRQB	31	32	NC	-	-	-	
	-	TBD	O	DAB1	33	34	CBLIDB#	I	-		
	-	TBD	O	DAB0	35	36	DAB2	O	TBD	-	
	-	TBD	O	HDCSB0#	37	38	HDCSB1#	O	TBD	-	
	-	-	I	HDACTB#	39	40	GND	PWR	-	-	

4.6 Serial ATA harddisk interface

Two serial ATA harddisk controllers are available on the board – a primary controller (SATA0) and a secondary controller (SATA1).

4.6.1 SATA Hard Disk Connector (SATA0, SATA1)

SATA0, J16:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA0 TX+				
3	SATA0 TX-				
4	GND	PWR	-	-	
5	SATA0 RX-				
6	SATA0 RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

SATA0 RX+ SATA0 RX-	Host transmitter differential signal pair
SATA0 TX+ SATA0 TX-	Host receiver differential signal pair

All of the above signals are compliant to [4].

SATA1, J15:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA1 TX+				
3	SATA1 TX-				
4	GND	PWR	-	-	
5	SATA1 RX-				
6	SATA1 RX+				
7	GND	PWR	-	-	

The signals used for the secondary Serial ATA harddisk interface are the following:

SATA1 RX+ SATA1 RX-	Host transmitter differential signal pair
SATA1 TX+ SATA1 TX-	Host receiver differential signal pair

All of the above signals are compliant to [4].

4.7 Floppy Disk Connector (FDC1)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	1	2	DENSEL0#	OC	/48	-	
	-	-	PWR	GND	3	4	NC	-	-	-	
	-	-	PWR	GND	5	6	DS1#	-	-	-	
	-	-	PWR	GND	7	8	INDEX#	IS	-	330R	
	-	-	PWR	GND	9	10	MOTEA#	OC	/48	-	
	-	-	PWR	GND	11	12	DRVB#	OC	/48	-	
	-	-	PWR	GND	13	14	DRVA#	OC	/48	-	
	-	-	PWR	GND	15	16	MOTEB#	OC	/48	-	
	-	-	PWR	GND	17	18	DIR#	OC	/48	-	
	-	-	PWR	GND	19	20	STEP#	OC	/48	-	
	-	-	PWR	GND	21	22	WDATA#	OC	/48	-	
	-	-	PWR	GND	23	24	WGATE#	OC	/48	-	
	-	-	PWR	GND	25	26	TRK0#	IS	-	330R	
	-	-	PWR	GND	27	28	WPT#	IS	-	330R	
				NC	29	30	RDATA#	IS	-	330R	
	-	-	PWR	GND	31	32	SIDE1#	OC	/48	-	
				NC	33	34	DSKCHG#	IS	-	330R	

Signal Description:

RDATA#	Read Disk Data, active low, serial data input from the floppy disk drive.
WDATA#	Write Disk Data, active low, serial data output to the floppy disk drive.
WGATE#	This output signal enables the head of the selected disk drive to write to the disk.
MOTEA#	This output signal enables the motor in floppy disk drive A.
MOTEB#	This output signal enables the motor in floppy disk drive B.
DRVA#	Active low output signal to select floppy disk drive A.
DRVB#	Active low output signal to select floppy disk drive B.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	This signal controls the direction of the floppy disk drive head movement during a seek operation. A low level request steps through centre.
STEP#	This output signal supplies step pulses to move the head during seek operations.
DENSEL0#	This output indicates whether a low data rate (250/300kbps at low level) or a high data rate (500/1000kbps at high level) has been selected.
TRK0#	Floppy Disk Track 0, active low input to indicate that the head of the selected drive is at track 0.
INDEX#	Floppy Disk Index, active low input indicates the beginning of a disk track.
WPT#	Active low input signal indicating that the selected drive contains a write protected disk.
DSKCHG#	Input pin that senses whether the drive door has been opened or the diskette has been changed.

4.8 Printer Port Connector (PRINTER).

The printer port connector is provided in a standard DB25 pinout.
The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1						
						14	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	2						
						15	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	3						
						16	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	4						
						17	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	5						
						18	GND	PWR	-	-	
	2K2	24/24	IO	PD4	6						
						19	GND	PWR	-	-	
	2K2	24/24	IO	PD5	7						
						20	GND	PWR	-	-	
	2K2	24/24	IO	PD6	8						
						21	GND	PWR	-	-	
	2K2	24/24	IO	PD7	9						
						22	GND	PWR	-	-	
	2K2	-	I	ACK#	10						
						23	GND	PWR	-	-	
	2K2	-	I	BUSY	11						
						24	GND	PWR	-	-	
	2K2	-	I	PE	12						
						25	GND	PWR	-	-	
	2K2	-	I	SLCT	13						

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

4.9 Serial Ports

Two RS232 serial ports (EIA/TIA-232-E compliant) are available on the 886LCD/ATX(GV) and 886LCD/ATXU(GV).

The typical interpretation of the signals in the COM ports is as follows:

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.9.1 Serial Port Com1 DB9 Connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5						
						9	RI	I	-	-	
	-		O	DTR	4						
						8	CTS	I	-	-	
	-		O	TxD	3						
						7	RTS	O		-	
	-	-	I	RxD	2						
						6	DSR	I	-	-	
	-	-	I	DCD	1						

4.9.2 Serial Port Com2 Pin Header Connectors.

The pinout of Serial ports Com2 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	RxD	I	-		
		-	I	TxD	3	4	DTR	O		-	
	-		O	GND	5	6	DSR	I	-		
	-		O	RTS	7	8	CTS	I	-		
	-	-	PWR	RI	9	10	NC		-	-	

If the DB9 adapter (ribbon cable) is used, the DB9 pinout will be identical to the pinout of Serial Com1

4.10 Ethernet connector.

The 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards supports 1 channel of 10/100Mb Ethernet using the Realtek 8100C LAN controller.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB LAN networks.

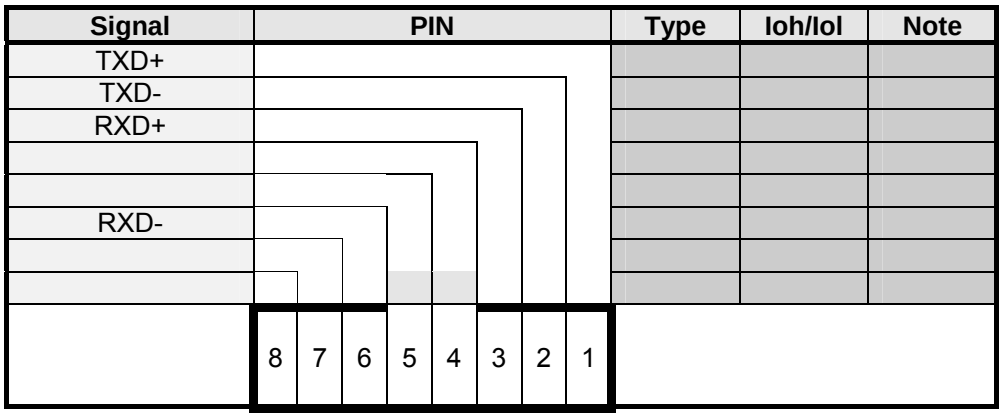
The signals for the Ethernet ports are as follows:

TXD+	Transmit pair in 10Base-T and 100Base-TX mode.
TXD-	
RXD+	Receive pair in 10Base-T and 100Base-TX mode.
RXD-	

4.10.1 Ethernet connector (ETHER)

The Ethernet connector is mounted together with USB Ports 4 and 5.

The pinout of the RJ45 connector is as follows:



4.11 USB Connector (USB)

The 886LCD/ATX(GV) and 886LCD/ATXU(GV) contains three USB (Universal Serial Bus) ports UHCI Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of 6 USB ports.

The USB Host Controllers support the standard Universal Host Controller Interface (UHCI) Specification, Rev 1.1. All 6 USB ports support both USB1.0 and USB2.0 signaling.

Over-current detection on all six USB ports is supported.

USB Port 0 and 1 are supplied on the separate Rear IO connector. USB Port 4 and 5 are supplied on the combined ETHER, USB4, USB5 connector. USB Ports 2 and 3 are supplied on the USB2/3 connector.

4.11.1 USB Connector 0/1 (USB0/1)

USB0 and USB 1 are located on a separate Rear IO connector (I/O Bracket connector).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB1-		USB1+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB v.1.1 standard, the 5V input supply must be at least 5.00V.

USB0+ USB0- USB1+ USB1-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.11.2 USB Connector 2/3 (USB2/3).

USB2 and USB3 are located on a a 2x5 pinrow connector.

The pinout of the USB2/3 connector (USB2) is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
1			PWR	5V/SB5V	1	2	5V/SB5V	PWR			1
	/15K	0.25/2	IO	USB2-	3	4	USB3-	IO	0.25/2	/15K	
	/15K	0.25/2	IO	USB2+	5	6	USB3+	IO	0.25/2	/15K	
			PWR	GND	7	8	GND	PWR			
			PWR	GND	9	10	NC				

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB v.1.1 standard, the 5V input supply must be at least 5.00V.

USB2+ USB2- USB3+ USB3-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.11.3 USB Connector 4/5 (USB4/5)

USB4 and USB5 are mounted together with ETHER ethernet port on a Rear IO connector (I/O Bracket connector).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB v.1.1 standard, the 5V input supply must be at least 5.00V.

USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.12 Audio Connector

4.12.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector.

IN	Signal	Type	Note
TIP	Line in – Left	IA	1
RING	Line in – Right	IA	1
SLEEVE	GND	PWR	
TIP	Line out – Left	OA	
RING	Line out – Right	OA	
SLEEVE	GND	PWR	
TIP	Mic1	IA	1
RING			
SLEEVE	GND	PWR	

Note 1: Signals are shorted to GND internally in the connector, when jack-plug is not inserted.

4.12.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	

CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

4.13 Fan connectors, CPU FAN, CHASSIS FAN, PWR FAN.

The **CPU FAN (FAN3)** is used for connection of the active cooler for the CPU.

The **CHASSIS FAN (FAN2)** can be used to power, control and monitor a fan for chassis ventilation etc.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	SENSE		-	1K	
2	12V_PWM	PWR	-	-	
3	GND	PWR	-	-	

Signal description:

12V_PWM	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 1000 mA can be supplied from this pin.
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 1K to +5V. The signal has to be pulses, typically 2 Hz per rotation.

The **PWR FAN (FAN1)** can be used for high power fans.

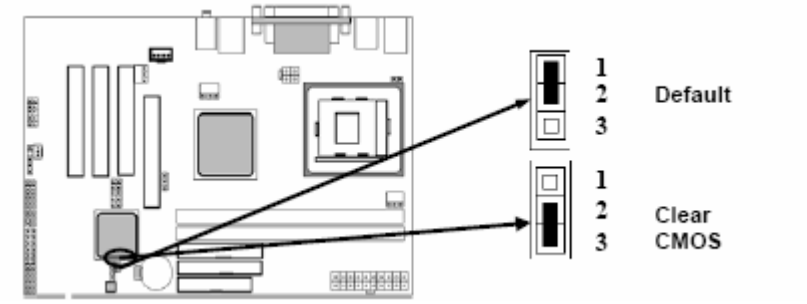
PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	SENSE		-	1K	
2	12V	PWR	-	-	
3	GND	PWR	-	-	

Signal description:

12V	+12V supply for fan. A maximum of 2000 mA can be supplied from this pin.
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 1K to +5V. The signal has to be pulses, typically 2 Hz per rotation.

4.14 The Clear CMOS Jumper, Clr-CMOS.

The Clear CMOS Jumper is used to clear the CMOS content.

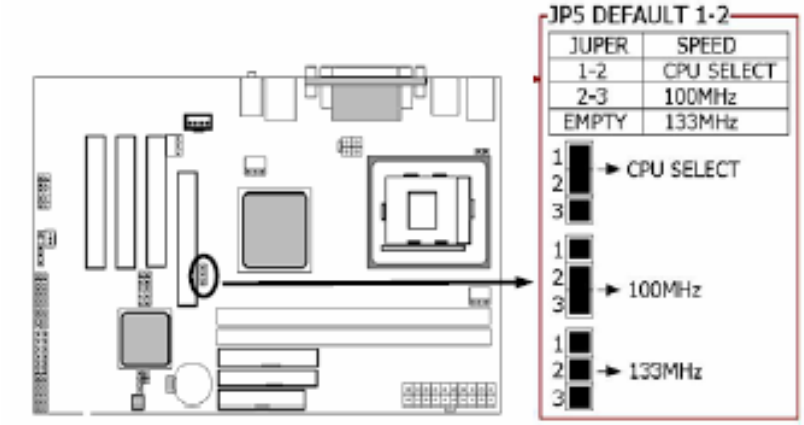


To clear all CMOS settings, including Password protection, move the Clear CMOS jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

4.15 Front Side Bus Speed, FSB

Select CPU base clock to one of 3 options by configuring the FSB jumper row (JP5) as shown below.



The CPU used has itself output signals that indicate what the maximum/default frequency to be used is. Please also note that the CPU internal clock multiplier is fixed by the manufacturer.

"CPU select": Will let the CPU / BIOS automatically control the base clock (default).

"100MHz setting": Will force CPU input clock to 100MHz and the internal CPU clock and FSB will be set accordingly.
CPU clock = 100MHz x Clock multiplier
FSB clock = 400MHz

"133MHz setting": Will force CPU input clock to 133MHz and the internal CPU clock and FSB will be set accordingly.
CPU clock = 133MHz x Clock multiplier
FSB clock = 533MHz

4.16 Case Open, S1

The Case Open connector can be used for Intrusion Detection. If Case is opened the switch should be closed.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
			PWR	GND	1	2	CASEOPEN#	I		220K	

4.17 Trusted Platform Module (TPM) connector, CN7 (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
			CLK	CLK_33MHz	1	2	GND	PWR			
				LFRAME#	3	4	NC				
				LRESET#	5	6	5V/SB5V	PWR			
				LAD3	7	8	LAD2				
			PWR	VCC3	9	10	LAD1				
				LAD0	11	12	GND	PWR			
				SMCLK	13	14	SMDATA				
			PWR	VCC3SB	15	16	GPIO				
			PWR	GND	17	18	SERIRQ				
				SUS_STAT#	19	20	LDRQ#				

4.18 Front Panel connector, CN5.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	330		PWR	GRN LED+	1	2	PWR LED+	PWR		330	
	330		PWR	GRN LED+	3	4	PWR LED+	PWR		330	
			O	GRN LED-	5	6	GND	PWR			
	330		PWR	HDD LED+	7	8	KBLOCK#	I			
			O	HDD LED-	9	10	GND	PWR			
			O	HDD LED-	11	12	SLEEP#	I			
	330		PWR	HDD LED+	13	14	GND	PWR			
			I	RESET#	15	16	+5V	PWR			
			PWR	GND	17	18	GND	PWR			
			I	PWRSW	19	20	GND	PWR			
			PWR	5V/SB5V	21	22	SPKR	O			

Signal	Description
GRN LED	Green Status LED. When the system is in Suspend, the green LED will flash. When the system is in normal working mode, the Green LED will be Off.
PWR LED	ATX Power LED. LED for showing ATX Power On
HDD LED	HDD LED for showing SATA or PATA activity
KBLOCK#	Keyboard Lock Switch. Active low signal will cause keyboard to be locked
SLEEP#	Suspend Switch Connector.
RESET#	Reset Switch Connector.
PWRSW	ATX Power Switch Connector
5V/SB5V	Standby 5V or ATX Power 5V depending on power state.
SPKR	Chassis Speaker Connector

4.19 GAME / MIDI Connector, CN6

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
			PWR	VCC	1	2	VCC	PWR			
				J1BUTTON1	3	4	J2BUTTON1				
				J1X	5	6	J2X				
			PWR	GND	7	8	MIDI_OUT				
			PWR	GND	9	10	J2Y				
				J1Y	11	12	J2BUTTON2				
				J1BUTTON2	13	14	MIDI_IN				
			PWR	VCC	15	16	NC				

Signal	Description
J1BUTTON1	Active-low, Joystick I switch input 1
J2BUTTON1	Active-low, Joystick II switch input 1
J1X	Joystick I timer pin. This pin connect to X positioning variable resistors for the Joystick
J2X	Joystick II timer pin. This pin connect to X positioning variable resistors for the Joystick
J1Y	Joystick II timer pin. This pin connect to Y positioning variable resistors for the Joystick
J2Y	Joystick I timer pin. This pin connect to Y positioning variable resistors for the Joystick
J1BUTTON2	Active-low, Joystick II switch input 2. This pin has an internal pullup resistor
J2BUTTON2	Active-low, Joystick I switch input 2. This pin has an internal pullup resistor
MIDI_IN	MIDI serial data input

4.20 IR Connector (IR1).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN
			PWR	VCC	1
				NC	2
			I	IRRX	3
			PWR	GND	4
			O	IRTX	5

Signal	Description
IRRX	Infrared receive signal. Support IrDA version 1.0 SIR Protocol with maximum baudrate up to 115.2 K bps
IRTX	Infrared transmit signal Support IrDA version 1.0 SIR Protocol with maximum baudrate up to 115.2 K bps

4.21 WOL Connector (W.O.L).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN
			PWR	5V/SB5V	1
			PWR	GND	2
			I	PME#	3

Signal	Description
PME#	Wake on LAN from an external LAN adapter is supported through this signal. Connect the W.O.L. signals from the adapter to this connector and install software to support W.O.L.
5V/SB5V	Standby 5V or ATX Power 5V depending on power state.

4.22 JP3 (optional).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN
			I	R-NTC	1
			I	R-NTC	2

Signal	Description
R-NTC	Option for connection of external temperature sensor based on NTC Resistor 150mW 10Kohm or simialar.

4.23 PCI Slot 1, Slot 2 and Slot 3 connectors.

4.23.1 PCI Slot Connector

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
		SOLDER SIDE			**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

4.23.2 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

4.23.3 886LCD/ATX(GV) and 886LCD/ATXU(GV) PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
886LCD/ATXU(GV)	1	AD16	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	2	AD17	INT_PIRQ#G	INT_PIRQ#F	INT_PIRQ#E	INT_PIRQ#H
	3	AD18	INT_PIRQ#C	INT_PIRQ#D	INT_PIRQ#B	INT_PIRQ#A
886LCD/ATX(GV)	1	AD16	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	2	AD17	INT_PIRQ#G	INT_PIRQ#F	INT_PIRQ#E	INT_PIRQ#H
	3	AD18	INT_PIRQ#C	INT_PIRQ#D	INT_PIRQ#B	INT_PIRQ#A
	4	AD19	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#A	INT_PIRQ#D
	5	AD23	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G
	6	AD25	INT_PIRQ#E	INT_PIRQ#H	INT_PIRQ#G	INT_PIRQ#F

5. System Resources

5.1 Memory map

The table below lists the system memory map.

Address range (hex)		Size	Description
00000000-	0007FFFF	512 Kbytes	Conventional memory
00080000-	0009FBFF	127 Kbyte	Extended conventional memory
0009FC00-	0009FFFF	1 Kbyte	Extended BIOS data
000A0000-	000AFFFF	64 Kbytes	845 VGA Controller, Video memory and BIOS
000B0000-	000BFFFF	64 Kbytes	845 VGA Controller, Video memory and BIOS
000C0000-	000CBFFF	48 Kbytes	845 VGA Controller, Video memory and BIOS
000CC000-	000CDFFF	8 Kbytes	Realtek 8100 Ethernet boot.
F0000000-	F7FFFFFF	0x8000000	845 VGA Controller
FEC00000-	FEC00FFF	0x1000	Motherboard resource (APIC)
FEE00000-	FEE00FFF	0x1000	Motherboard resource (APIC)
FF8FF800-	FF8FF8FF	0x100	Realtek 8100 Ethernet Controller
FF8FFC00-	FF8FFDFF	0x200	SATA/RAID controller
FFA7F400-	FFA7F7FF	0x400	USB Controller
FFA7F800-	FFA7F8FF	0x100	Realtek AC97 Audio
FFA7FC00-	FFA7FDFF	0x200	Realtek AC97 Audio
FFA80000-	FFAFFFFF	0x80000	845 VGA Controller
FFB7FC00-	FFB7FFFF	0x400	Ultra SATA Controller
FFB80000-	FFBFFFFF	0x80000	Intel 82802 Firmware Hub Device
FFC00000-	FFF7FFFF	0x380000	Motherboard reserved
FFF80000-	FFFFFFFF	0x80000	Intel 82802 Firmware Hub Device

5.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
0	0	0	8086	2560		MCH	Northbridge
0	2	0	8086	2562		MCH	Graphics
0	29	0	8086	24C2		ICHS	USB
0	29	1	8086	24C4		ICHS	USB
0	29	2	8086	24C7		ICHS	USB
0	29	7	8086	24CD		ICHS	USB
0	30	0	8086	244E		ICHS	PCI to PCI bridge
0	31	0	8086	24C0		ICHS	ISA/LPC Bridge
0	31	1	8086	24CB		ICHS	IDE Controller
0	31	3	8086	24C3		ICHS	SMBUS Controller
0	31	5	8086	24C5		ICHS	Audio Device
1	0	-	-	-	AD16	-	PCI SLOT 1
1	1	-	-	-	AD17	-	PCI SLOT 2
1	2	-	-	-	AD18	-	PCI SLOT 3
1	3	-	-	-	AD19	-	PCI SLOT 4
1	4	0	1095	3512	AD20	SIL3512	SATA Controller
1	5	0	10EC	8139	AD21	RTL8100	Ethernet
1	7	-	-	-	AD23	-	PCI SLOT 5
1	9	-	-	-	AD25	-	PCI SLOT 6

Note: All PCI slots for the 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards support PCI BUS Mastering.

5.3 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard SATA controller	May be used by onboard Parallel Port	May be used by onboard Floppy disk Controller	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used by primary harddisk controller	May be used by secondary harddisk controller	May be used for onboard Sound System	May be used by onboard USB controller	May be used by onboard Ethernet controller	May be used by onboard VGA Controller	May be used by onboard SMBus Controller	Available on PCI slots as IRQA-IRQH depending on selections in the BIOS	Notes
NMI	•																				
IRQ0		•																			
IRQ1			•																		
IRQ2				•																	
IRQ3						•														•	1,2
IRQ4					•															•	1,2
IRQ5							•	•							•	•	•	•	•	•	1,2
IRQ6									•												
IRQ7							•	•							•	•	•	•	•	•	1,2
IRQ8										•											
IRQ9							•								•	•	•	•	•	•	1,2
IRQ10							•								•	•	•	•	•	•	1,2
IRQ11							•								•	•	•	•	•	•	1,2
IRQ12											•										
IRQ13												•									
IRQ14													•							•	1
IRQ15														•						•	1
IRQ16																•		•			3
IRQ17															•	•			•		3
IRQ18																•	•				3
IRQ19							•														3
IRQ20																•					3
IRQ21																					3
IRQ22																					3
IRQ23																					3

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQH can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ16 to IRQ23 are APIC interrupts

5.4 I/O Map

Address (hex)	Size	Description
0020- 0021	2	Programmable interrupt controller
0040- 0043	4	System Timer
0060- 0060	1	Standard keyboard
0061- 0061	1	System speaker
0070- 0071	2	System CMOS/Real time clock
0170- 01F7	8	Secondary Parallel ATA IDE Channel
01F0- 01F7	8	Primary Parallel ATA IDE Channel
02F8- 02FF	8	Comport 2
0378- 037F	8	Printer Port
03B0- 03BB	0xC	845 VGA Controller
03C0- 03DF	0x20	845 VGA Controller
03F8- 03FF	8	Comport 1
0CF8- 0CFF	8	PCI Bus
D000- D0FF	0x100	Realtek 8100 Ethernet Controller
D400- D40F	0x10	SATA/Raid Controller
D480- D483	4	SATA/Raid Controller
D800- D807	8	SATA/Raid Controller
D880- D883	4	SATA/Raid Controller
DC00- DC07	8	SATA/Raid Controller
E000- E01F	0x20	Standard Universal PCI to USB Host Controller
E080- E09F	0x20	Standard Universal PCI to USB Host Controller
E400 E41F	0x20	Standard Universal PCI to USB Host Controller
E480- E49F	0x20	PCI System Management Bus
E800- E8FF	0x100	Realtek AC97 Audio
EC00- EC3F	0x40	Realtek AC97 Audio
FFA0- FFAF	0x10	Ultra ATA Controller

5.5 DMA Channel Usage

DMA Channel Number	Data Width	System Resources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

6. Overview of BIOS features

This Manual section details specific BIOS features for the 886LCD/ATX(GV) and 886LCD/ATX(GV) boards. The BIOS are based on the AMI BIOS core version 8 with Kontron BIOS extensions.

6.1.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
• BIOS data, such as the BIOS revision level
• Fixed-system data, such as peripherals, serial numbers, and asset tags
• Resource data, such as memory size, cache size, and processor speed
• Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

The 886LCD Boards support reading certain MIF specific details by the Windows API. Refer to the API section in this manual for details.

6.1.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

7. BIOS Configuration / Setup

7.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the 886LCD/ATX(GV) and 886LCD/ATXU(GV) boards. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins.

The Menu bar is shown below:

```
                              BIOS Setup Utility
  Main     Advanced     PCIPnP     Boot     Security     Chipset     Power     Exit
```

The available keys for the Menu screens are as follows:

Function Key	Description
<←> or <→>	Select Screen
<↑> or <↓>	Select Item
<+> or <->	Change Field
<Tab>	Select Field
<F1>	General Help
<F10>	Save and Exit
<Esc>	Exits the Menu

The following section lists the available BIOS setup information and features of the different Menus.

7.2 Main Menu

```
                              BIOS Setup Utility
  Main     Advanced     PCIPnP     Boot     Security     Chipset     Power     Exit
  System Overview                                    Use [ENTER], [TAB] or
                                                     [SHIFT-TAB] to select a
  AMIBIOS                                            field.
  Version    : 08.00.10
  Build Date: 10/18/05                               Use [+] or [-] to
  ID         : 886AT014                              configure system Time.
  PCB ID     : 01
  Serial #   : 00375748
  Part   #   : 66610000



  Processor
  Type       : Intel(R) Pentium(R) 4 CPU 2.4GHZ
  Speed      : 2400MHz                               <-   Select Screen
  Count      : 1                                     ||   Select Item
                                                     +-   Change Field
  System Memory                                      Tab  Select Field
  Size       : 1016MB                                F1   General Help
                                                     F10  Save and Exit
  System Time                    [10:18:15]          ESC  Exit
  System Date                    [Mon 03/15/2006]
            V02.53 (C)Copyright 1985-2002, American Megatrends, Inc.
```

Main Menu Selections

Feature	Options	Description
System Time	HH:MM:SS	Set the system time
System Date	MM/DD/YYYY	Set the system date

7.3 Advanced Menu

```
                              BIOS Setup Utility
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
  Advanced Settings                                  Configure CPU.

  Warning: Setting wrong values in below sections
           May cause system to malfunction.

> CPU Configuration
> IDE Configuration
> Floppy Configuration
> SuperIO Configuration
> Hardware Health Configuration
> ACPI Configuration
> USB Configuration

                                                     <-    Select Screen
                                                     ||    Select Item
                                                     Enter Go to Sub
                                                     Screen
                                                     F1    General Help
                                                     F10   Save and Exit
                                                     ESC   Exit
          V02.53 (C)Copyright 1985-2002, American Megatrends, Inc.
```

7.3.1 Advanced settings – CPU Configuration

```
                              BIOS Setup Utility
                 Advanced
  Configure advanced CPU settings                    This should be
                                                     enabled in order to
  Manufacturer: Intel                                boot legacy OSes that
  Brand String: Intel (R) Pentium(R) CPU 2.40GHz     cannot Support CPUs
  Frequency   : 2.40GHz                              with Extended CPUID
  FSB Speed   : 533MHz                               Functions.

  Cache L1    : 8 KB
  Cache L2    : 512 KB

  Ratio Status       :Locked
  Ratio Actual Value :18
    Ratio CMOS Setting:              [18]
    VID CMOS Setting  :              [62]            <-    Select Screen
                                                     ||    Select Item
  Max CPUID Value Limit:             [Disabled]      +-    Change Option
                                                     F1    General Help
                                                     F10   Save and Exit
                                                     ESC   Exit
          V02.53 (C)Copyright 1985-2002, American Megatrends, Inc.
```

Feature	Options	Description
Max CPUID Value Limit	**Disabled**, Enabled	This should be enabled in order to boot legacy OSes that cannot Support CPUs with Extended CPUID Functions.

7.3.2 Advanced settings – IDE Configuration

```
                              BIOS Setup Utility
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
 IDE Configuration                                  DISABLED: disables
                                                    the integrated IDE
 OnBoard PCI IDE Controller   [Both]                Controller.
                                                    PRIMARY: enables only
                                                    The Primary IDE
 Primary IDE Master                : [Hard Disk]    Controller.
 Primary IDE Slave                 : [Not Detected] SECONDARY: enables
 Secondary IDE Master              : [Not Detected] Only the Secondary
 Secondary IDE Slave               : [Not Detected] IDE
                                                    Controller.
 Hard Disk Write Protect         [Disabled]         BOTH: enables both
 IDE Detect Time Out (Sec)       [35]               IDE
 ATA(PI) 80Pin Cable Detection   [Host & Device]    Controllers.


                                                    <-    Select Screen
                                                    ||    Select Item
                                                    +-    change option
                                                    F1    General Help
                                                    F10   Save and Exit
                                                    ESC   Exit

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```
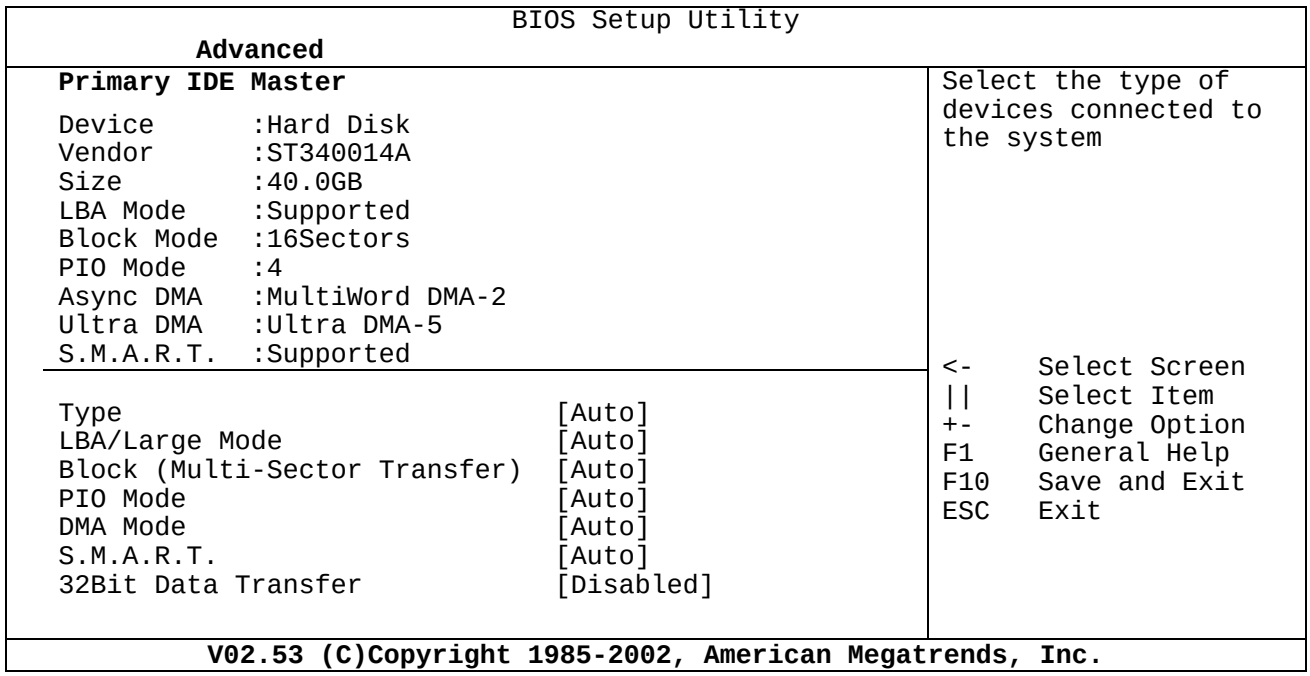
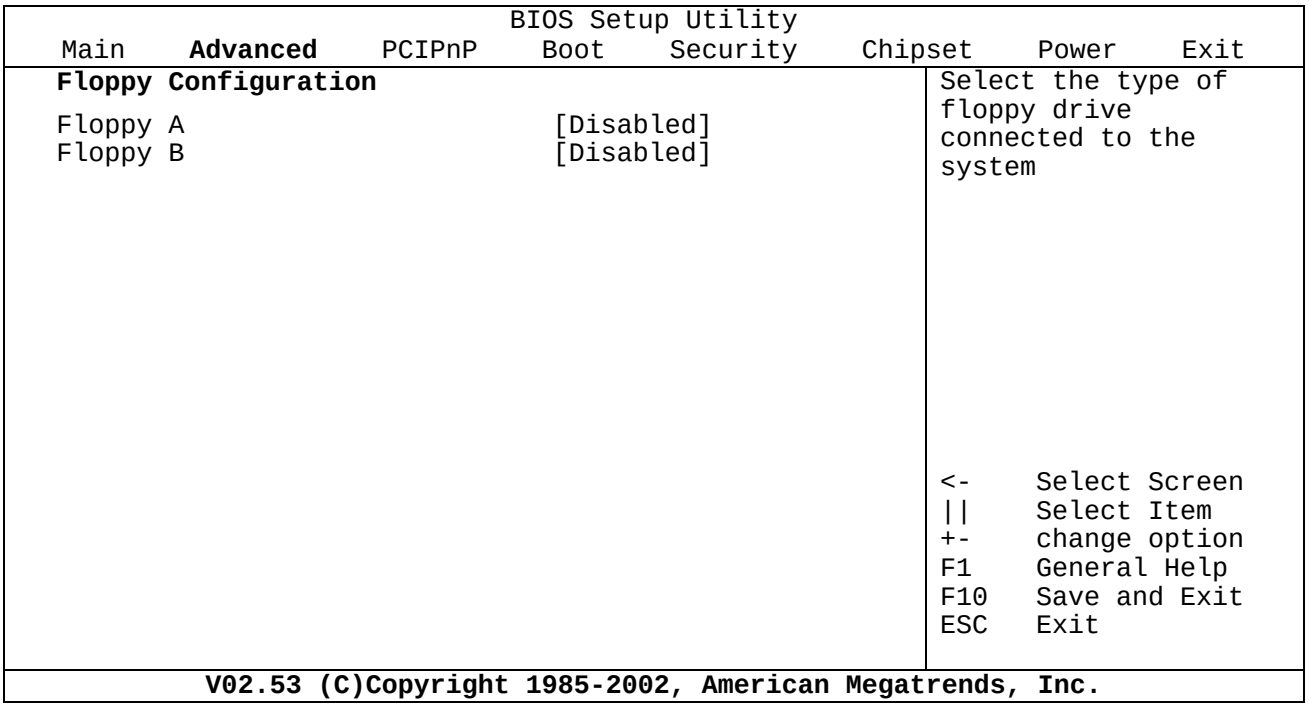

Feature	Options	Description
OnBoard PCI IDE Controller	Disabled, Primary, Secondary, **Both**	Setup the configuration of the hard drive interfaces.
Hard Disk Write Protect	**Disable**, Enabled	Enable write protection on HDDs, only works when it is accessed through the BIOS.
IDE Detect Time Out (Sec)	0, 5, 10, 15, 20, 25, 30, **35**	Select the time out value when the BIOS is detecting ATA/ATAPI Devices.
ATA(PI) 80Pin Cable Detection	**Host & Device**, Host, Device	Select the mechanism for detecting 80Pin ATA Cable.



Feature	Options	Description
Type	Not Installed, **Auto,** CDROM, ARMD	Select the type of device connected to the system.
LBA/Large Mode	Disabled, **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled, **Auto**	Select if the device should run in Block mode.
PIO Mode	**Auto**, 0, 1, 2, 3, 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	**Auto**, SWDMA0, SWDMA1, SWDMA2, MWDMA0, MWDMA1, MWDMA2, UDMA0, UDMA1, UDMA2, UDMA3, UDMA4, UDMA5	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Note: To use UDMA Mode 2, 3, 4 and 5 with a device, the harddisk cable used MUST be UDMA66 cable (80 conductor cable).**
S.M.A.R.T.	**Auto**, Disabled, Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System).
32Bit Data Transfer	**Disabled**, Enabled	Select if the Device should be using 32Bit data Transfer.

7.3.3 Advanced settings – Floppy Configuration

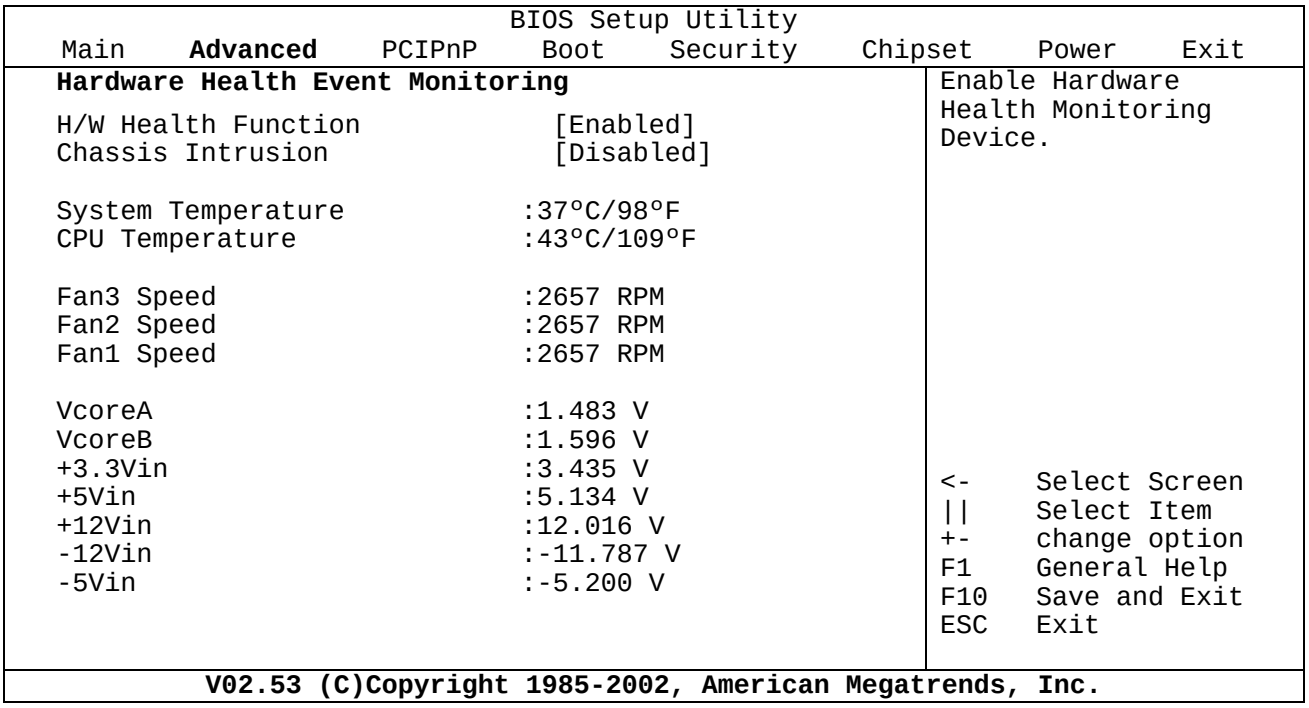

BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
Floppy Configuration
Floppy A [Disabled]
Floppy B [Disabled]
Select the type of floppy drive connected to the system
<- Select Screen
|| Select Item
+- change option
F1 General Help
F10 Save and Exit
ESC Exit
V02.53 (C)Copyright 1985-2002, American Megatrends, Inc.

Feature	Options	Description
Floppy A	**Disabled,** 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB	Select Floppy device installed in the system.
Floppy B	**Disabled**, 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB	Select Floppy device installed in the system.

7.3.4 Advanced settings – SuperIO Configuration

```
                        BIOS Setup Utility
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
 Configure Win627THF Super IO Chipset          | Allows BIOS to Enable
                                               | or Disable Floppy
 OnBoard Floppy Controller      [Disabled]     | Controller.
 Floppy Drive Swap              [Disabled]     |
 Serial Port1 Address           [3F8/IRQ4]     |
 Serial Port2 Address           [2F8/IRQ3]     |
   Serial Port2 Mode            [Normal]       |
 Parallel Port Mode             [Disabled]     |
 OnBoard Game Port              [Disabled]     |
                                               |
                                               |
                                               
```

7.3.5 Advanced settings – Hardware Health Configuration



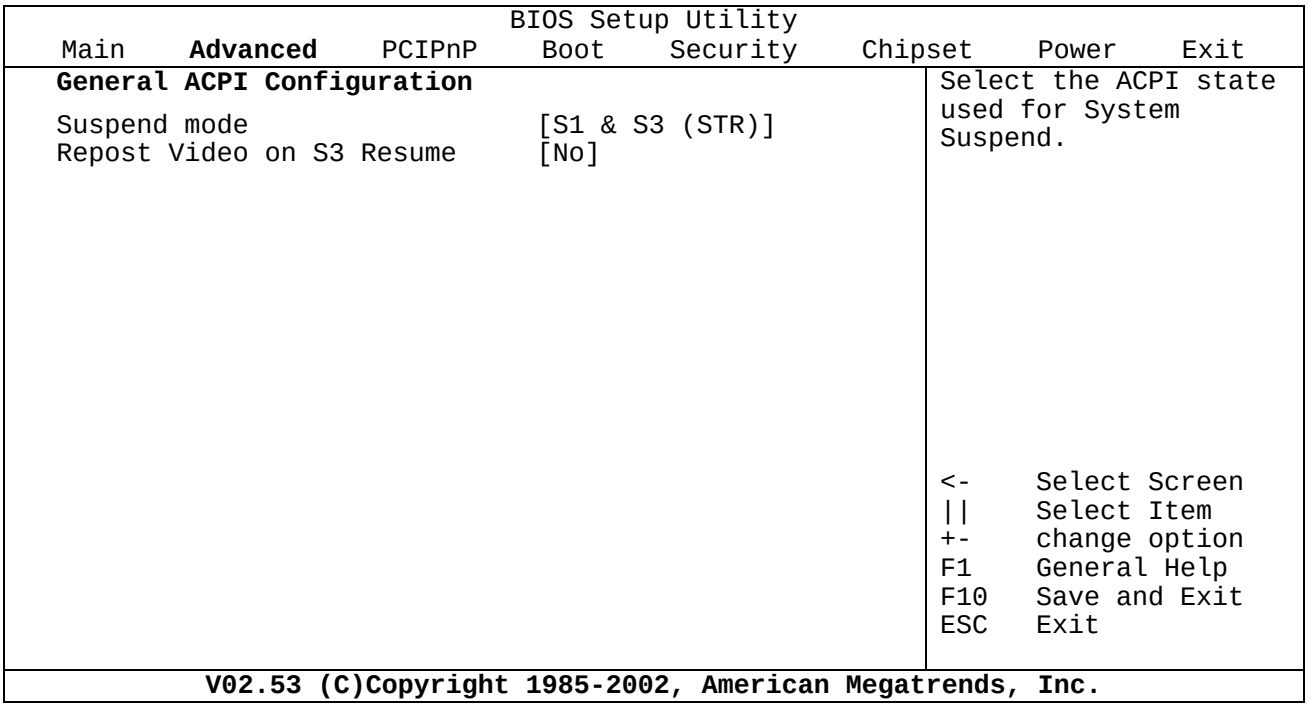
Feature	Options	Description
H/W Health Function	**Enable,** Disabled	Enable Hardware Health Monitoring Device .
Chassis Intrusion	Enable, **Disabled**	Enable BIOS warning in case intrusion is detected on Case Open (S1).

7.3.6 Advanced settings – ACPI Configuration

```
                              BIOS Setup Utility
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
  ACPI Aware O/S                [Yes]                  Enable / disable
                                                       ACPI support for
> General ACPI Configuration                           Operating System
> Advanced ACPI Configuration
                                                       ENABLE: IF OS
                                                       supports ACPI.

                                                       DISABLE: IF OS does
                                                       not support ACPI.



                                                       <-    Select Screen
                                                       ||    Select Item
                                                       +-    change option
                                                       F1    General Help
                                                       F10   Save and Exit
                                                       ESC   Exit
          V02.53 (C)Copyright 1985-2002, American Megatrends, Inc.
```

Feature	Options	Description
ACPI Aware O/S	No, **Yes**	Select if O/S supports ACPI.

7.3.7 Advanced settings – General ACPI Configuration

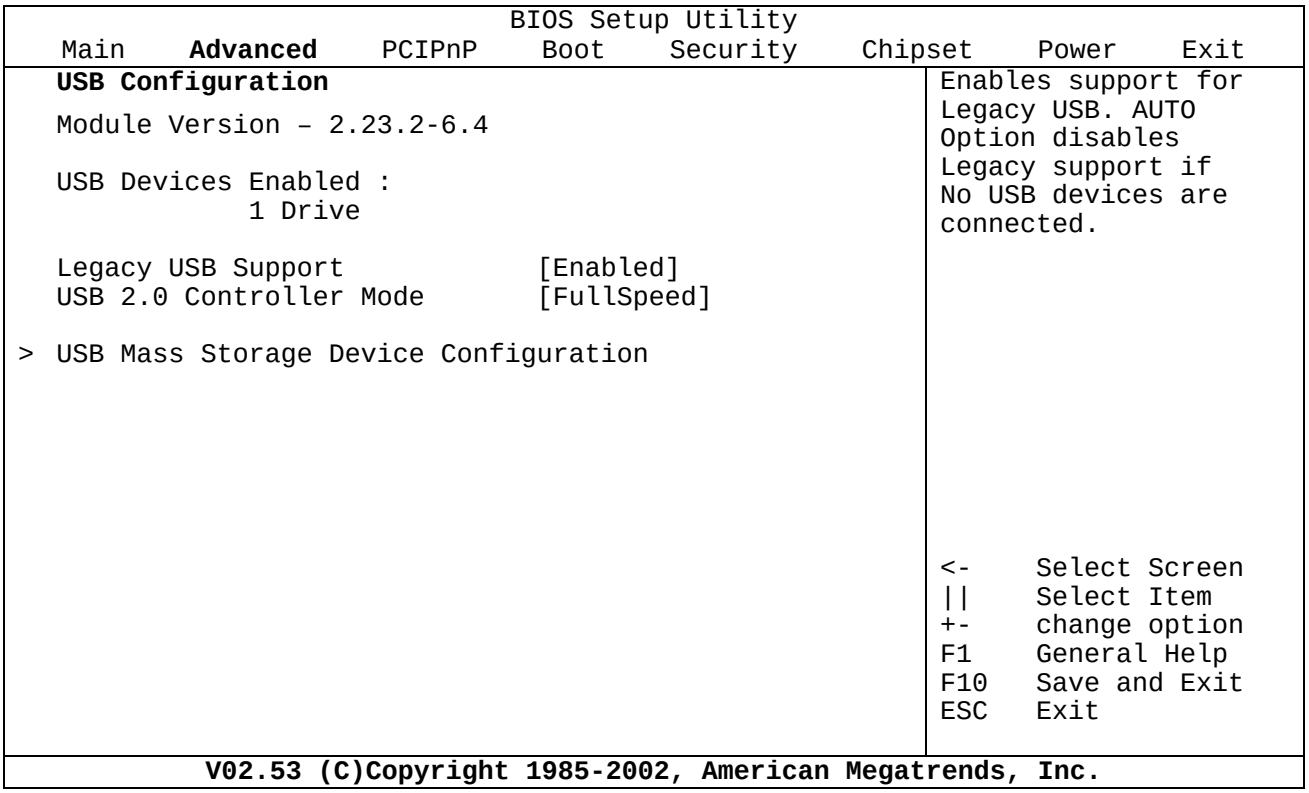

BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
General ACPI Configuration
Suspend mode [S1 & S3 (STR)]
Repost Video on S3 Resume [No]
Select the ACPI state used for System Suspend.
<- Select Screen
|| Select Item
+- change option
F1 General Help
F10 Save and Exit
ESC Exit
V02.53 (C)Copyright 1985-2002, American Megatrends, Inc.

Feature	Options	Description
Suspend mode	S1 (POS) only, **S1&S3 (STR**)	Select the ACPI state used for System Suspend.
Repost Video on S3 Resume	**No**, Yes	Determines whether to invoke VGA BIOS post on S3/STR resume.

7.3.8 Advanced settings – Advanced ACPI Configuration

```
                         BIOS Setup Utility
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
 Advanced ACPI Configuration                  | Enable RSDP pointers
                                              | to 64-bit Fixed
 ACPI 2.0 Features              [No]          | System Description
 ACPI APIC support              [Enabled]     | Tables.
 AMI OEMB table                 [Enabled]     |
 Headless mode                  [Disabled]    |
                                              |
                                              |
                                              
```

7.3.9 Advanced settings – USB Configuration


BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
USB Configuration
Module Version – 2.23.2-6.4
USB Devices Enabled :
1 Drive
Legacy USB Support [Enabled]
USB 2.0 Controller Mode [FullSpeed]
> USB Mass Storage Device Configuration
Enables support for Legacy USB. AUTO Option disables Legacy support if No USB devices are connected.
<- Select Screen
|| Select Item
+- change option
F1 General Help
F10 Save and Exit
ESC Exit
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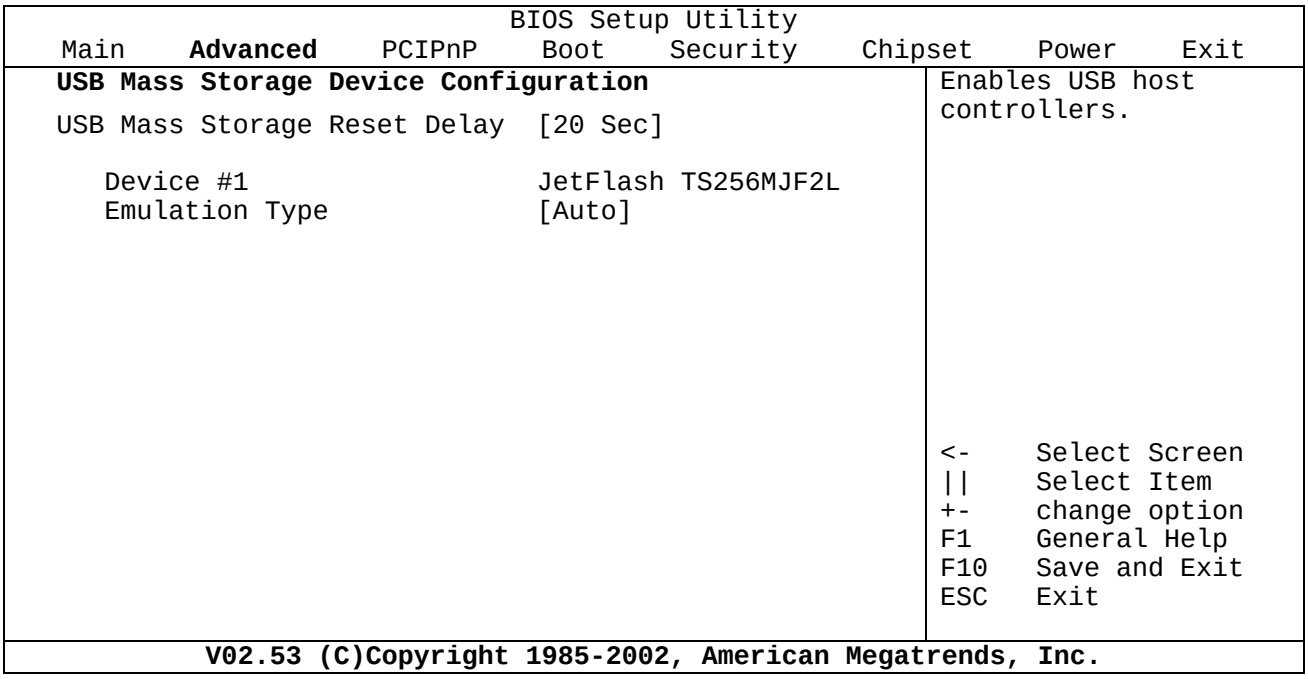
Feature	Options	Description
Legacy USB Support	Disabled, **Enabled**, Auto	Support for legacy USB Keyboard.
USB 2.0 Controller Mode	**FullSpeed**, HiSpeed	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).

7.3.10 Advanced settings – USB Mass Storage Device Configuration


BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
USB Mass Storage Device Configuration
USB Mass Storage Reset Delay [20 Sec]
Device #1 JetFlash TS256MJF2L
Emulation Type [Auto]
Enables USB host controllers.
<- Select Screen
|| Select Item
+- change option
F1 General Help
F10 Save and Exit
ESC Exit
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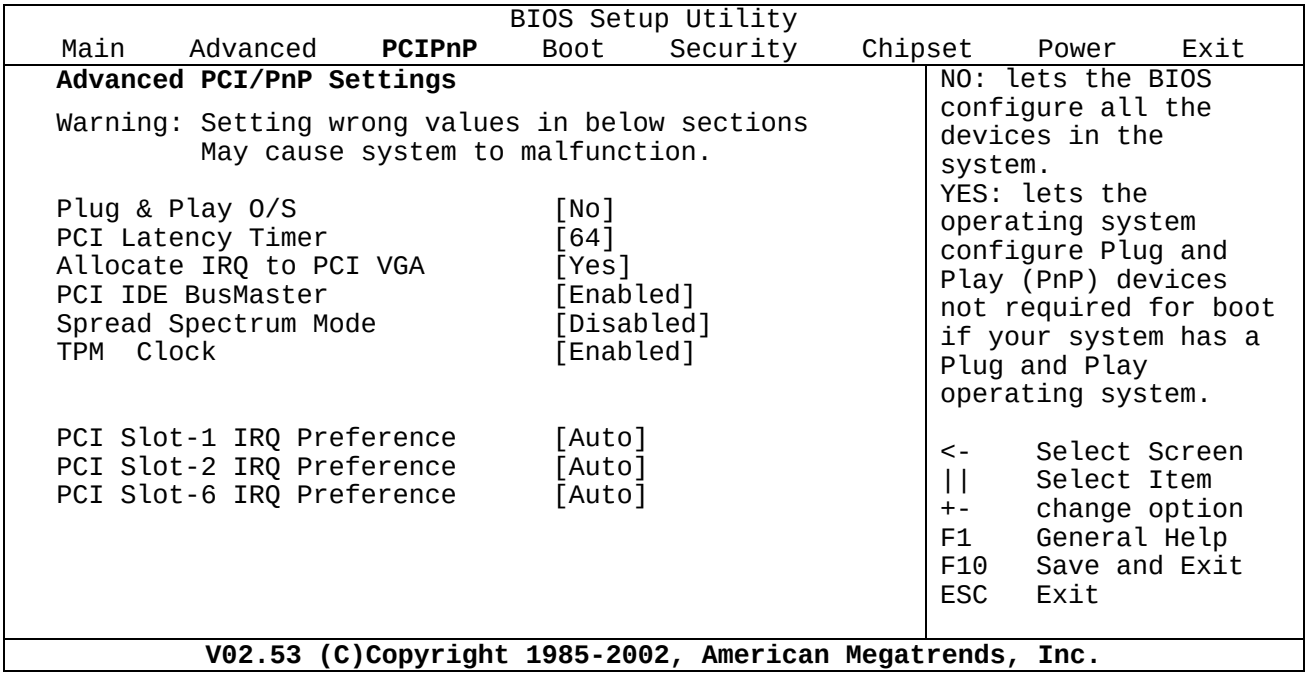
Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec, **20 Sec**, 30 Sec, 40 Sec	Number of seconds the BIOS waits for the USB device after start unit command.
Emulation Type	**Auto**, Floppy, Forced FDD, Hard Disk, CDROM	Setup the emulation type for the USB device.

7.4 PCIPnP Menu


BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
Advanced PCI/PnP Settings
Warning: Setting wrong values in below sections
May cause system to malfunction.
Plug & Play O/S [No]
PCI Latency Timer [64]
Allocate IRQ to PCI VGA [Yes]
PCI IDE BusMaster [Enabled]
Spread Spectrum Mode [Disabled]
TPM Clock [Enabled]
PCI Slot-1 IRQ Preference [Auto]
PCI Slot-2 IRQ Preference [Auto]
PCI Slot-6 IRQ Preference [Auto]
NO: lets the BIOS configure all the devices in the system.
YES: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.
<- Select Screen
|| Select Item
+- change option
F1 General Help
F10 Save and Exit
ESC Exit
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Feature	Options	Description
Plug & Play O/S	**No,** Yes	Select if you have a PnP O/S.
PCI Latency Timer	32, **64**, 96, 128, 160, 192, 224, 248	Value in units of PCI clocks for PCI device latency timer register.
Allocate IRQ to PCI VGA	**Yes**, No	Assigns IRQ to PCI VGA card.
Palette Snooping	**Disabled**, Enabled	ENABLED: informs the PCI device that an ISA graphics device is installed in the system so the card will function correctly.
PCI IDE BusMaster	**Enabled**, Disabled	Setup PCI bus mastering for read/write to IDE drives.
Spread Spectrum Mode	**Enabled**, Disabled	Spread Spectrum Mode.
PCI Slot-1 IRQ Preference	**Auto**, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Manual IRQ selection.
PCI Slot-2 IRQ Preference	**Auto**, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Manual IRQ selection.
PCI Slot-6 IRQ Preference	**Auto**, 3, 4, 5, 7, 9, 10, 11, 12, 14, 15	Manual IRQ selection. Only available on the 886LCD/ATX(GV)

Note: PCI Slot-3 IRQ Preference, PCI Slot-4 IRQ Preference and PCI Slot-5 IRQ Preference do not exist.

7.5 Boot Menu

```
                              BIOS Setup Utility
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
  Boot Settings                                    Configure Settings
                                                   during System Boot.
> Boot Settings Configuration

  1st Boot Device                  [PM-ST3120022A]
  2nd Boot Device                  [1st FLOPPY DRIVE]
  3rd Boot Device                  [CORSAIR Flash Voya]
  4th Boot Device                  [Realtek Boot Agent]

                                                   <-    Select Screen
                                                   ||    Select Item
                                                   Enter Go to Sub
                                                   Screen
                                                   F1    General Help
                                                   F10   Save and Exit
                                                   ESC   Exit

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```

7.5.1 Boot – Boot Settings Configuration

```
                              BIOS Setup Utility
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
 Boot Settings                                    Configure Settings
                                                  during System Boot.

 Quick Boot                        [Enabled]
 Quiet Boot                        [Disabled]
 AddOn ROM Display Mode            [force BIOS]
 Bootup Num-Lock                   [On]
 PS/2 Mouse Support                [Auto]
 Wait for `F1´ If Error            [Enabled]
 Hit 'DEL' Message Display         [Enabled]
 Interrupt 19 Capture              [Disabled]

                                                  <-    Select Screen
                                                  ||    Select Item
                                                  Enter Go to Sub
                                                  Screen
                                                  F1    General Help
                                                  F10   Save and Exit
                                                  ESC   Exit

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```

Feature	Options	Description
Quick Boot	**Enabled**, Disabled	Allows BIOS to skip certain test while booting.
Quiet Boot	**Disabled**, Enabled, Enabled & Maintain	Shows boot logo instead of POST screen.
AddOn ROM Display Mode	**Force BIOS**, Keep Current	Set display mode for Option ROM.
Bootup Num-Lock	Off, **On**	Select Power-on state for numlock.
PS/2 Mouse Support	Disabled, Enabled, **Auto**	Select support for PS/2 Mouse.
Wait For ´F1´If Error	**Enabled**, Disabled	Wait for F1 key to be pressed if error occurs. (See note 1 below)
Hit 'DEL' Message Display	Disabled, **Enabled**	Display the message or not.
Interrupt 19 Capture	**Disabled**, Enabled	Allows option ROMs to trap interrupt 19.

Note 1: Errors: <INS> Pressed, Timer Error, Interrupt Controller-1 error, Keyboard/Interface Error, Primary Master Hard Disk Error, S.M.A.R.T HDD Error, Cache Memory Error, DMA Controller Error, Resource Conflict, PCI I/O conflict, PCI ROM conflict, PCI IRQ conflict, PCI IRQ routing table error, Halt on Invalid Time/Date, NVRAM Bad, Static Resource Conflict, PCI I/O conflict and PCI ROM conflict.

7.6 Security Menu

```
                              BIOS Setup Utility
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
 Security Settings                                  Install or Change the
                                                    password.

 Supervisor Password :Installed
 User Password       :Installed

 Change Supervisor Password
 User Access Level               [Full Access]
 Change User Password
 Clear User Password
 Password Check                  [Setup]

 Boot Sector Virus Protection    [Disabled]

 Hard Disk Security                                 <-    Select Screen
                                                    ||    Select Item
 Primary Master HDD User Password                   Enter Go to Sub
 Primary Slave HDD User Password                    Screen
 Secondary Slave HDD User Password                  F1    General Help
                                                    F10   Save and Exit
                                                    ESC   Exit
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```

Feature	Options	Description
Change Supervisor Password	Password	Change the Supervisor Password.
User Access Level	No Access, View Only, Limited, Full Access	Set the user level Access for the BIOS.
Change User Password	Password	Change the User Password.
Clear User Password	Ok, Cancel	Clears the User Password.
Password Check	Setup, Always	Shall the BIOS prompt for password on boot or only when entering setup.
Boot Sector Virus Protection	Enabled, **Disabled**	Will write protect the MBR when the BIOS is used to access the harddrive.
HDD Password	Password	Locks the HDD with a password, the user needs to type the password on power on.

7.7 Chipset Menu

```
                              BIOS Setup Utility
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
  Advanced Chipset Settings                        Intel Brookdale-G
                                                   NorthBridge chipset
  Warning: Setting wrong values in below sections  configuration
  may cause system to malfunction.                 options.

> Intel Brookdale-G NorthBridge Configuration
> Intel ICH4 SouthBridge Configuration

                                                   <-    Select Screen
                                                   ||    Select Item
                                                   Enter Go to Sub
                                                   Screen
                                                   F1    General Help
                                                   F10   Save and Exit
                                                   ESC   Exit

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```
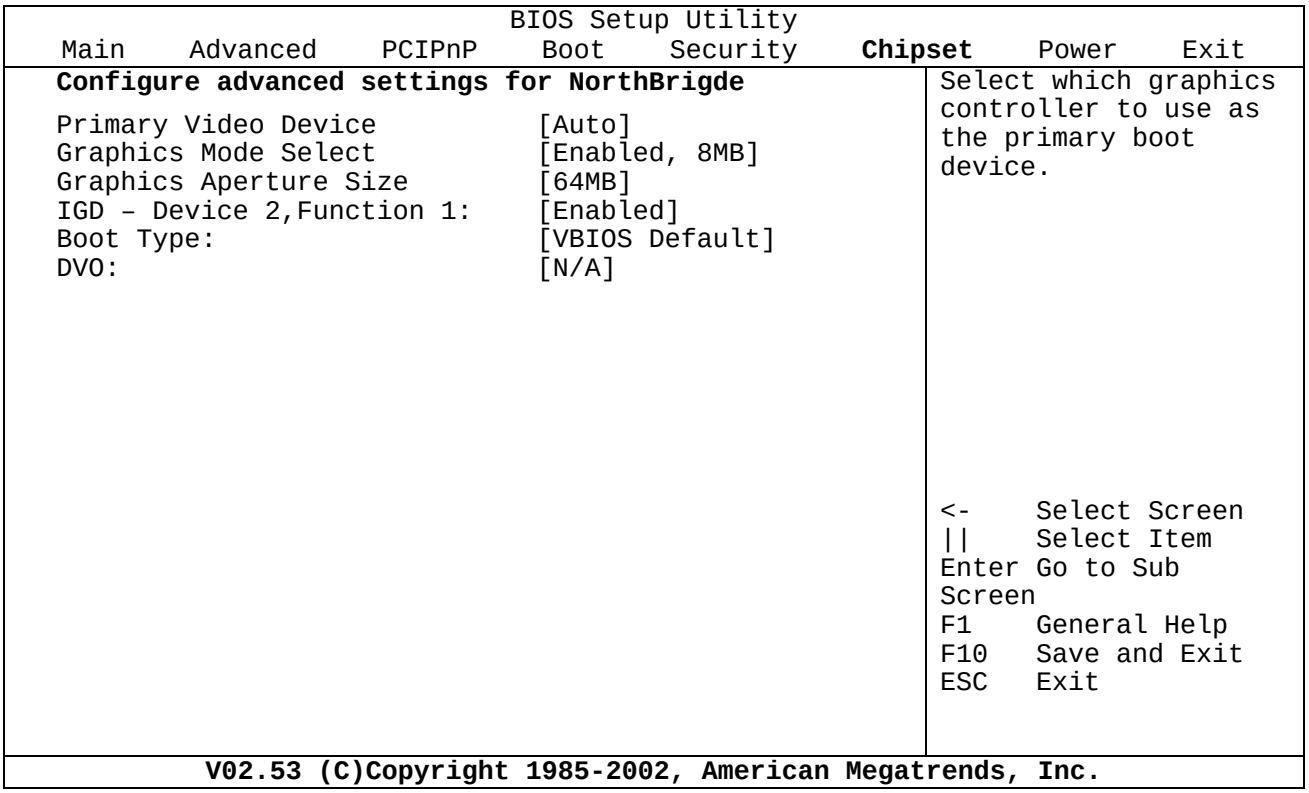

7.7.1 Advanced Chipset Settings – Intel Brookdale-G NorthBridge Configuration


BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
Configure advanced settings for NorthBrigde
Primary Video Device [Auto]
Graphics Mode Select [Enabled, 8MB]
Graphics Aperture Size [64MB]
IGD – Device 2,Function 1: [Enabled]
Boot Type: [VBIOS Default]
DVO: [N/A]
Select which graphics controller to use as the primary boot device.
<- Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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Feature	Options	Description
Primary Video Device	Internal, External PCI, **Auto**	Select which graphics controller to use as the primary boot device.
Graphics Mode Select	Disabled, 1MB, 4MB, **8MB**, 16MB, 32MB	Select the amount of system memory used by the internal graphics device.
Graphics Aperture Size	4MB, 8MB, 16Mb, 32MB, **64MB**, 128MB, 256MB	Size of the AGP Aperture memory.
IGD – Device 2, Function 1	Disabled, **Enabled**	Setup the multimonitor function.
Boot Type	**VBIOS Default**, CRT, LFP, CRT+LFP, EFP, TV, CRT+EFP, CRT+TV, EFP+EFP2, EFP+TV	Setup type of boot screen.
DVO	[N/A]	

7.7.2 Advanced Chipset Settings – SouthBridge Configuration

```
                        BIOS Setup Utility
 Main   Advanced   PCIPnP   Boot   Security   Chipset   Power   Exit
                                                  Enable / Disable the
                                                  ICH4 IOAPIC function.

 Onboard IDE                  [Enabled]
 SMBUS                        [Enabled]
 AC´97 Audio                  [Enabled]
 USB #1                       [Enabled]
 USB #2                       [Enabled]
 USB #3                       [Enabled]
 EHCI (USB 2.0)               [Enabled]


 Onboard LAN                  [Enabled]
 Onboard SATA                 [Enabled]
 IOAPIC                       [Enabled]
 Extended IOAPIC              [Enabled]
                                                  <-    Select Screen
                                                  ||    Select Item
                                                  Enter Go to Sub
                                                  Screen
                                                  F1    General Help
                                                  F10   Save and Exit
                                                  ESC   Exit

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```
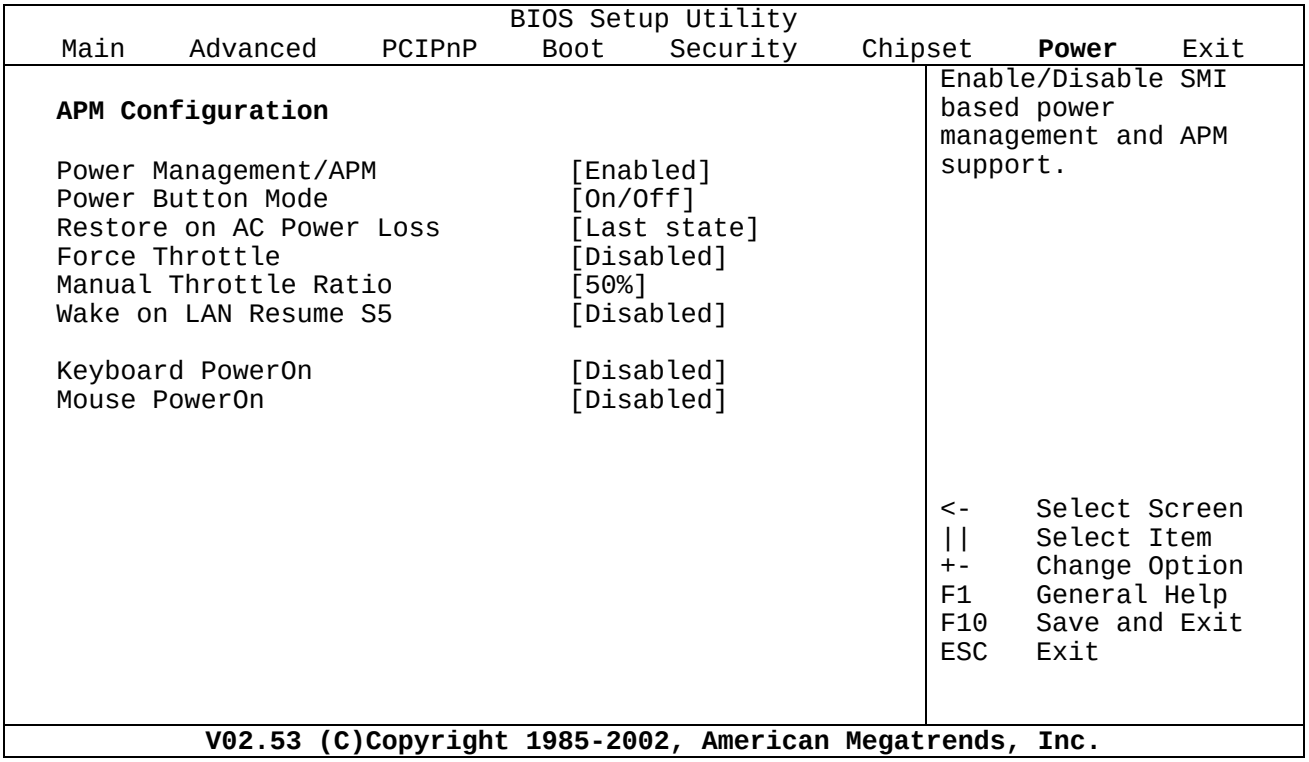

Feature	Options	Description
Onboard IDE	**Enabled** Disable	Enable / Disable ICH4 IDE Controller function.
SMBUS	**Enabled** Disable	Enable / Disable ICH4 SMBUS function.
AC´97 Audio	**Enabled** Disable	Enable / Disable ICH4 AC97 Audio Controller function.
USB #1	**Enabled** Disable	Enable / Disable ICH4 USB Host Controller#1 function.
USB #2	**Enabled** Disable	Enable / Disable ICH4 USB Host Controller#2 function.
USB #3	**Enabled** Disable	Enable / Disable ICH4 USB Host Controller#3 function.
EHCI (USB 2.0)	**Enabled** Disable	Enable / Disable ICH4 EHCI USB Controller function.
Onboard LAN	Disable **Enabled** With RPL/PXE boot	Set up Onboard LAN for Disable, Enable or Enable with RPL/PXE boot.
Onboard Sata	**Enabled** Disable	Enable / Disable Onboard SATA.
IOAPIC	**Enabled** Disable	Enable / Disable the ICH4 IOAPIC function.
Extended IOAPIC	**Enabled** Disable	Enable / Disable the extended mode of ICH4 IOAPIC function.

7.8 Power Menu


BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
APM Configuration
Power Management/APM [Enabled]
Power Button Mode [On/Off]
Restore on AC Power Loss [Last state]
Force Throttle [Disabled]
Manual Throttle Ratio [50%]
Wake on LAN Resume S5 [Disabled]
Keyboard PowerOn [Disabled]
Mouse PowerOn [Disabled]
Enable/Disable SMI based power management and APM support.
<- Select Screen
|| Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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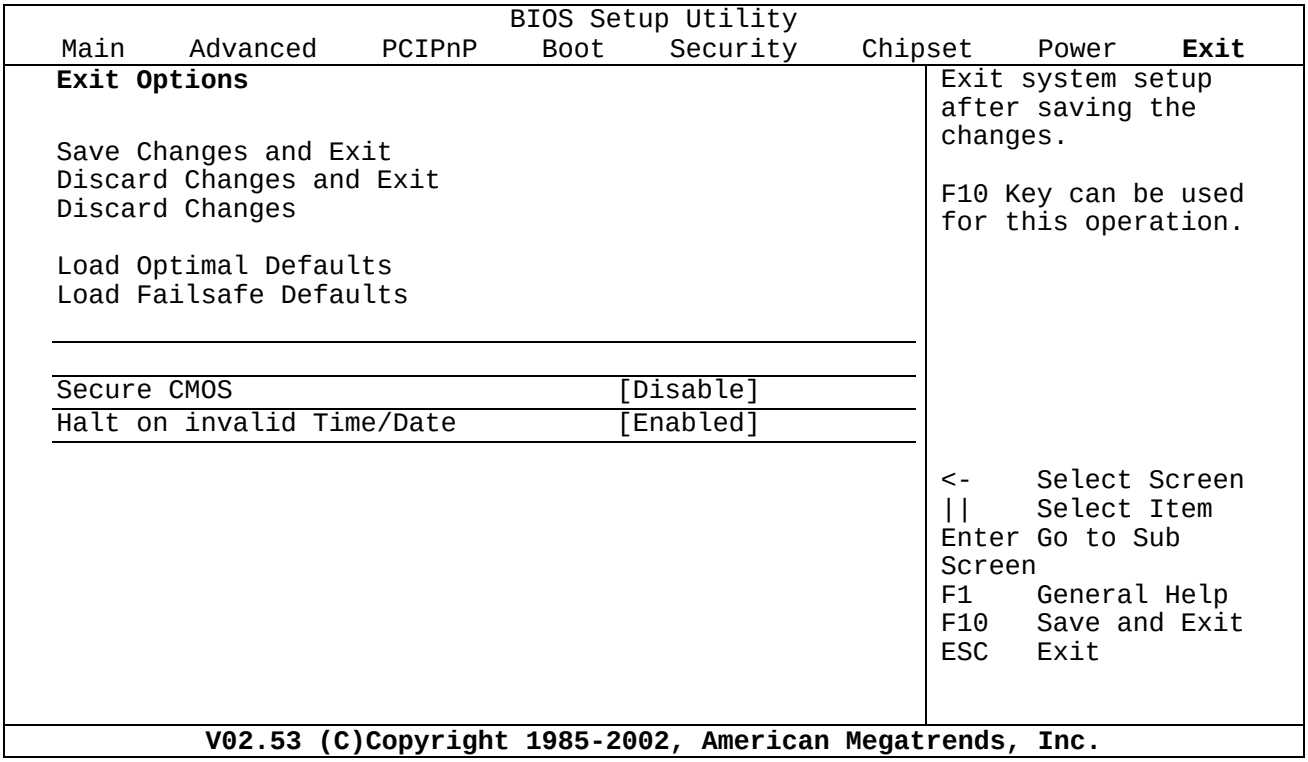
Feature	Options	Description
Power Management/APM	Disabled, **Enabled**	Setup the SMI/APM support.
Power Button Mode	**On/Off**, Standby, Suspend	Go Into On/Off, Standby or Suspend when Power button is pressed.
Restore on AC Power Loss	Power Off, Power On, **Last State**	
Force Throttle	**Disabled**, Enabled	Disable/Enable the force to thermal throtting function.
Manual Throttle Ratio	87.5%, 75.0%, 62.5%, **50%**, 37.5%, 25%, 12.5%	Select the Duty Cycle in Throttle mode.
Wake on LAN Resume S5	**Disabled**, Enabled	Disabled,Enabled generate of SMI on SLP_EN sp we can wake from S5.
Keyboard PowerOn	**Disabled**, Space Key	
Mouse PowerOn	**Disabled**, Double Left Button, Double Right Button	

7.9 Exit Menu


BIOS Setup Utility
Main Advanced PCIPnP Boot Security Chipset Power Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Secure CMOS [Disable]
Halt on invalid Time/Date [Enabled]
Exit system setup after saving the changes.
F10 Key can be used for this operation.
<- Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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Feature	Options	Description
Save Changes and Exit	Ok, Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok, Cancel	Exit system setup without saving any changes
Discard Changes	Ok, Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok, Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok, Cancel	Load Failsafe Default values for all the setup questions
Secure CMOS	**Disable**, Enabled	Enabled will store current CMOS in non volatile ram. This will maintain the settings even if battery is failing.
Halt on Invalid Time/Date	Disable, **Enabled**	

7.10 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

8. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on the 886LCD/ATXU(GV) and 886LCD/ATX(GV) Driver CD or they can be downloaded from the homepage http://www.kontron-emea.com

9. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
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2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.